# DESIGN OF FREQUENCY SYNTHESIZER

A THESIS SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIRMENTS
FOR THE
DEGREE OF

**MASTER OF TECHNOLOGY**
**IN**
**VLSI DESIGN & EMBEDDED SYSTEM**

By

**GAURAV KUMAR**
**Roll No: 212EC2135**


DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY
ROURKELA, ODISHA
INDIA
2012-2014

# DESIGN OF FREQUENCY SYNTHESIZER

A THESIS SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIRMENTS
FOR THE
DEGREE OF

**MASTER OF TECHNOLOGY**
**IN**
**VLSI DESIGN & EMBEDDED SYSTEM**

By

**GAURAV KUMAR**
**Roll No: 212EC2135**

Under the Guidance of

## Prof. D. P. ACHARYA


DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY
ROURKELA, ODISHA
INDIA
2012-2014


# National Institute Of Technology

# Rourkela

# CERTIFICATE

This is to certify that the thesis entitled, " **Design of Frequency synthesizer**" submitted by **Gaurav Kumar** in partial fulfilment of the requirements for the award of Master of Technology degree in Electronics and Communication Engineering with specialization in "**VLSI Design and Embedded system**" at the National institute of Technology, Rourkela is a study work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university / institute for the award of any degree diploma.

Date:

**prof. D. P. Acharya**

Dept. of Electronics and communication Engg.

National Institute Of Technology

Rourkela - 769008

# ACKNOWLEDGEMENTS

This project is by far the most significant accomplishment in my life and it would be impossible without people (especially my family) who supported me and believed in me.

I am thankful to **Prof. D. P. Acharya,** Professor in the department of Electronics and Communication Engineering, NIT Rourkela for giving me the opportunity to work under him and lending every support at every stage of this project work. I truly appreciate and value him esteemed guidance and encouragement from the beginning to the end of this thesis. I am indebted to his for having helped me shape the problem and providing insights towards the solution. His trust and support inspired me in the most important moments of making right decisions and I am glad to work with him.

I want to thank all my teachers **Prof. K.K. Mahapatra, Prof. P. K. Tiwari, Prof. A. K. Swain,** and **Prof. M. N. Islam** for providing a solid background for my studies and research thereafter.

GAURAV KUMAR

ROLL NO: 212EC2135

# CONTENTS

# ABSTRACT

PLL frequency synthesizers play an important role in communication field and continuously increases. Frequency synthesizer is a system that generate a set of frequency, which is an integer multiple of input frequency. After that fractional frequency synthesizer was inventesd. In which output frequency is fractional multiple of input frequency. They suddenly used in mobile communication and in spread spectrum applications and their use continuously increasing.

Communication used single carrier frequency, which is fixed. After modulation when modulating signal transmitted, then frequency of modulating signal will change because of noise. So at receiver to get the input signal, we require input carrier frequency so that we require frequency synthesizer.

PLL is closed loop frequency system that can be used as a frequency synthesizer and for synchronizing purpose. PLL's are having building block like, Phase frequency detector (PFD), charge pump, loop filter, voltage controlled oscillator (VCO). When it used as a frequency synthesizer than one another block require which is called divider circuit.

PFD compare input signal frequency and phase with feedback signal and generate UP and DOWN signal. Which drive charge pump, that convert two signal into one signal. That signal increase or decrease the charge of loop filter. By which output frequency of VCO will change, it may be increase or decrease depending on charge on loop filter. That output frequency ($f_{vco}$) applied to divider circuit, which divide the $f_{vco}$ by an number, that number may be integer or fractional. Output frequency of divider circuit compare with input frequency. If input frequency same as feedback frequency and phase error is zero then we say that PLL is locked, mean's frequency of input signal same as feedback signal and phase difference between is zero. After locked state, output of PFD is zero and charge on loop filter also constant, so $f_{vco}$ is constant. After that PLL track the input signal.

Here I used PLL as fractional frequency synthesizer. Which generate output frequency which is fractional multiple of input signal frequency.

# LIST OF FIGUERS

# ABBREVIATIONS USED

| | |
|---|---|
| PLL | Phase Locked Loop |
| PFD | Phase Frequency detector |
| CP | Charge Pump |
| LPF | Low Pass Filter |
| VCO | Voltage Controlled Oscillator |
| $V_{cont}$ | Control Voltage |
| $\zeta$ | Damping Factor |
| $K_D$ | Phase Frequency Detector and Charge pump Gain |
| K | VCO Gain |

# CHAPTER 1

# INTRODUCTION

## 1.1 System overview

PLL is closed loop frequency system that can be used as a frequency synthesizer and for synchronizing purpose. PLL's are having building block like, Phase frequency detector (PFD), charge pump, loop filter, voltage controlled oscillator (VCO). When it used as a frequency synthesizer than one another block require which is called divider circuit. PLL compare the frequency and phase of input signal with feedback signal, when phase error is constant and zero then PLL is locked. PLL compare the input signal with feedback signal until these signals are locked. If these two signal are not locked then error signal generated by PDF which increase and decrease the charge on loop filter. So output frequency of VCO may be speed up or down depending on error signal. This process continuous until the phase error between input signal and feedback signal is constant or zero then we will get locked state. After the locked state output of each block is constant. Now we get a signal which has same phase as input signal phase.

PLL having five main building blocks:

1. Phase Detector (PD) and Phase Frequency Detector (PFD)
2. Charge Pump (CP)
3. Loop Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
5. Divided By N.F

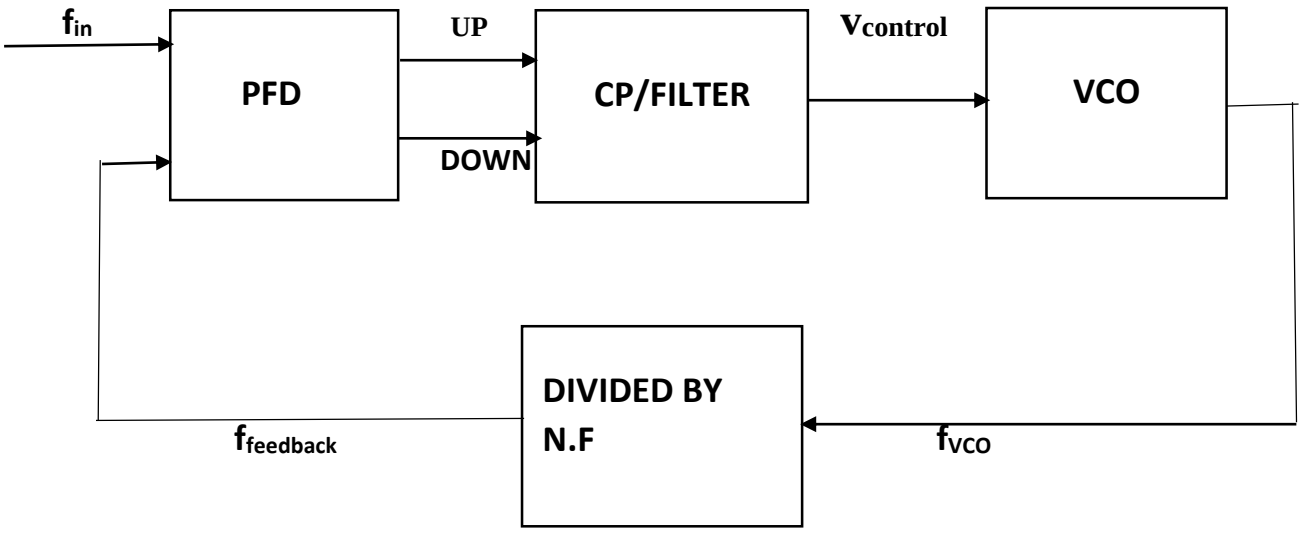



Figure 1. Block diagram of PLL as a frequency synthesizer [2]

Phase frequency detector (PFD) compare frequency and phase of input signal with feedback signal. If there is a phase difference between the two signals then PFD generate the UP and DOWN signals. These signal increase/decrease the charge on filter. Then that charge speed up/slow down the frequency of VCO. There is loop filter which is low pass filter (LPF). LPF can pass only low frequency and stop the high frequency, so we can say that output signal from LPF is dc signals which drive VCO. When UP signal generated by PFD, then charge pump pumps the charge onto the LPF capacitor, which increase the $v_{control}$. By which the frequency of VCO will speed be up. When DOWN signal generated by PFD then charge pump remove the charge from the LPF capacitor, which decrease the $v_{control}$. By which the frequency of VCO will be slow down. The output signal with frequency $f_{VCO}$ is applied to divide by N.F circuit, which divide the $f_{VCO}$ By N.F and output signal of this circuit applied to PFD which compare these two signals, if phase error between these two signals is constant or zero then phase get locked. Then frequency of VCO ($f_{VCO}$) is N.F times the frequency of input signal.

## 1.2 Literature Review

R.E.Best, "Phase-Locked Loops: Design, Simulation, and Applications", 3rd edition, New York: McGraw-Hill, 1997 in which he describe the types of the Phase frequency detector and working of all PFD. Also he tell about the advantage and disadvantage of all PFD. In this he also tell about the parameters of PLL and how to calculate all the parameters. He also tell about to how to design the PLL as a frequency synthesiser.

Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw-Hill Edition, 2002 in which he describe the effect of resistance in series with capacitor of loop filter by which system become stable and to reduce the ripples, he use another capacitor in parallel to the combination of the capacitor and resistance. He also describe the physics behind the voltage controlled oscillator and how to generate the periodic signals. He also tell about the charge pump and what is the effect of power supply on charge pump. To reduce this he used the pair of transistor in series.

Uma kanta nanda, "Design of a low noise PLL for GSM application", IEEE International conference 2013 in which he gives the concept of high speed phase frequency detector with low noise. He also tell about, how to design the low noise PLL. He also tell how to calculate the phase noise and how the phase noise vary with the frequency.

Behzad Razavi, "RF Microelectronics", Tata McGraw-Hill, 2nd edition, 1997 in which he tell about the divider circuit and gives the concept of double edge trigger flip flop. He also tell how to design the fast D latch by using the differential circuit but power dissipation will increase. He also tell how to design the fractional divider circuit and how to change the dividing ratio by which how is your circuit will change.

### 1.3. Thesis Description

This “phase locked loop design as a frequency synthesizer” final thesis contains seven chapter.

In each chapter contain introduction, how to design the schematic circuit and simulation of schematic circuit, results and conclusion.

Chapter 2, include the types of phase frequency detector, how phase frequency works and simulation of schematic circuit.

Chapter 3, include the charge pump. In which I describe how charge pump working then design the charge pump and find problem. Then design the modified charge pump and simulation of charge pump.

Chapter 4, include the loop filter in which I describe how loop filter effect the working of PLL and modified the loop filter circuit and simulate the circuit.

Chapter 5, include the voltage control oscillator in which I describe how VCO work and what is the basic behind the theory of VCO, then I design the circuit and simulate the circuit.

Chapter 6, include the divider circuit in which I describe how fractional divider working, then design the circuit and simulate the circuit.

Chapter 7, include the results and conclusions of the final circuit.

# CHAPTER 2

# PHASE FREQUENCY DETECTOR

## 2.1 INTRODUCTION

A phase frequency detector is a circuit that senses the input signal and feedback signal and delivering an output error signal that is proportional to the phase difference between input signal and feedback signal. In ideal case, the relation between output error signal and phase difference ($\Delta\Phi$) between input signal and feedback signal is linear. Output error signal is zero for $\Delta\Phi = 0$ and increasing with $\Delta\Phi$. A phase frequency detector generate the UP and DOWN signal as an output error signal. When output error signal is UP, then charge pump remove the charge from the capacitor of LPF, by which voltage across capacitor will increase, that voltage applied to VCO so frequency of VCO will be speed up. If output error signal is DOWN then charge pump remove the charge from capacitor of LPF, by which voltage across capacitor will decrease. That voltage is an input of VCO so frequency of VCO will be slow down.

So we can say that, if UP signal is generated then the frequency of VCO will be speed up and if DOWN signal is generated then the frequency of VCO will be slow down.

## 2.2 PHASE DETECTORS AND PHASE FREQUENCY DETECTOR

A Phase detector is a circuit that sense the phase difference between input signal and feedback signal and generate output error signal. There are few example of phase detector which given below:

1. Multiplier phase detector

2. EXOR phase detector

3. J-K phase detector

4. Phase frequency detector

## 1. Multiplier phase detectors

In multiplier phase detector is used to measure the phase difference between input signal and feedback signal and generate the output error signal. That is used mostly in liner PLL (LPLL).

In LPLL the input signal ($V_1$) is mostly a sine wave and given as [2]:

$$V_1(t) = V_{max1} \sin (w_1 t + \Theta_1) \quad \ldots\ldots 1$$

Where $V_{max1}$ amplitude of input signal, $w_1$ is signal frequency and $\Theta_1$ is signal phase.

The second input signal is a square wave ($V_2$) and given as:

$$V_2(t) = V_{max2} \text{ rect } (w_2 t + \Theta_2) \quad \ldots\ldots\ldots 2$$

To simplify the analysis, square signal express by fourier series and given as

$$V_2(t) = V_{max2} \left[ \frac{4}{\Pi} \sin (w_2 t + \Theta_2) + \frac{4}{3\Pi} \sin (3w_2 t + \Theta_2) + \ldots\ldots\ldots\ldots \right] \quad \ldots\ldots\ldots 3$$

The output error signal is obtain by multiplying the two input signals, therefor we get

$$V_d(t) = V_{max1} \sin (w_1 t + \Theta_1) . V_{max2} \left[ \frac{4}{\Pi} \sin (w_2 t + \Theta_2) + \frac{4}{3\Pi} \sin (3w_2 t + \Theta_2) + \ldots \right] \quad \ldots\ldots\ldots 4$$

When PLL is locked then input frequency will same ($w_1 = w_2$), then

$$V_d(t) = V_{max1} . V_{max2} \left[ \frac{2}{\Pi} \sin \Theta_e \right] \quad \ldots\ldots\ldots 5$$

As $\Theta_e = \Theta_1 - \Theta_2$ is the phase error. The first term is wanted 'dc' term, where as other higher frequency term stop by LPF. By taking $K_d = \frac{2Vmax1.Vmax2}{\Pi}$ and neglecting the higher frequency terms, we get

$$V_d(t) = K_d . \sin (\Theta_e) \quad \ldots\ldots\ldots 6$$

Where $k_d$ is detector gain. When phase error between input signals is small, we get

$$V_d(t) = K_d . \Theta_e \quad \ldots\ldots\ldots 7$$

This equation show the liner relation between output error signal and phase difference between two input signals of the multiplier phase detector. The dimension of $K_d$ is volt / rad [2].

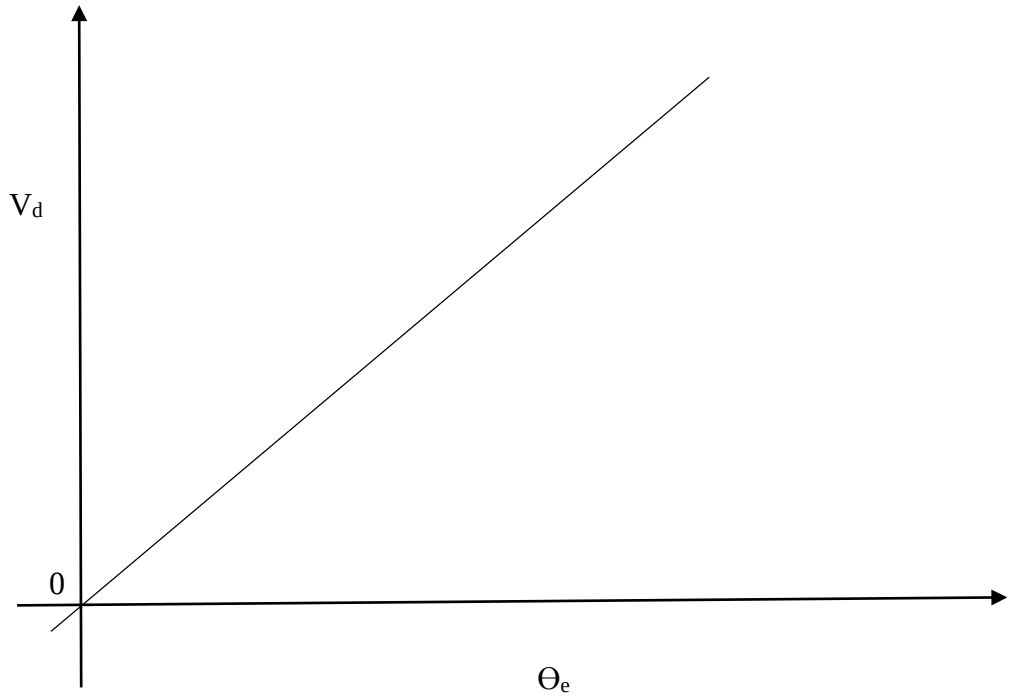



Figure 2.1 $V_d$ verse $\Theta_e$

## 2. EXOR phase detector

EXOR phase detectors are used mostly in digital PLL (DPLL). DPLL sense the phase difference between phase's of input signals and generate the output error signal which has liner relation with phase difference ($\Delta\Phi$) of input signals. The signals in DPLL are binary signal.

We analysis this phase detector for different values of $\Delta\Phi$.

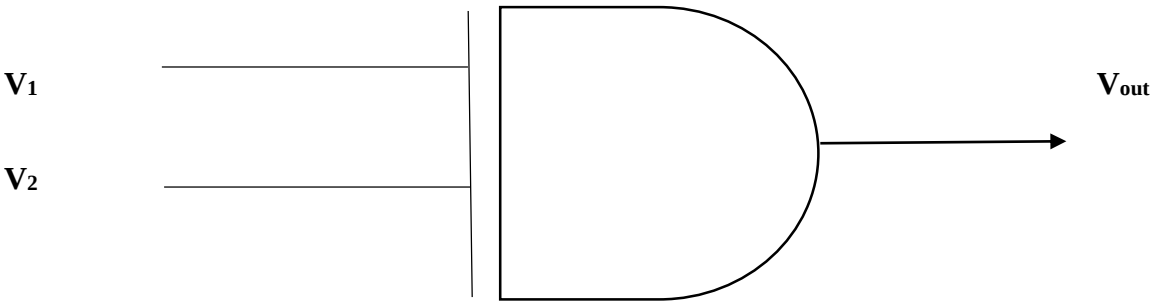



Fig. 2.2 EXOR phase detector

**(A).** when $\Delta\Phi = 0$ , then

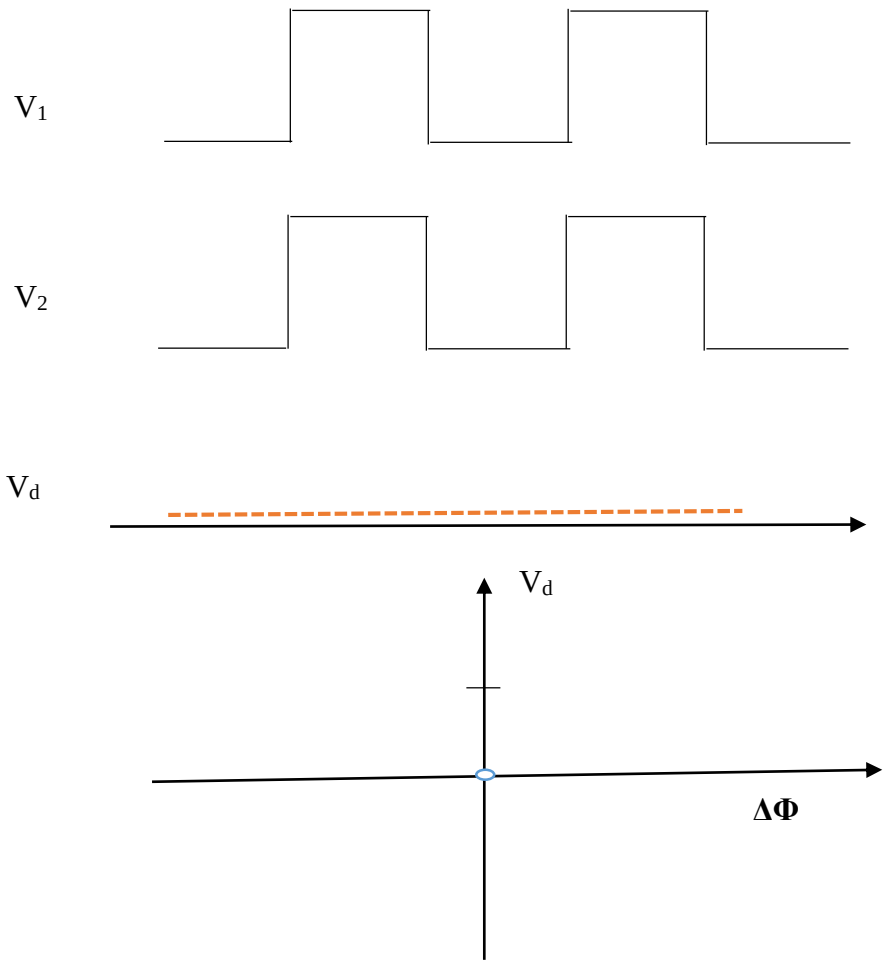



Fig 2.3. EXOR phase detector with $\Delta\Phi = 0$

**(B)**. When $\Delta\Phi = +/- \frac{\Pi}{2}$ , then

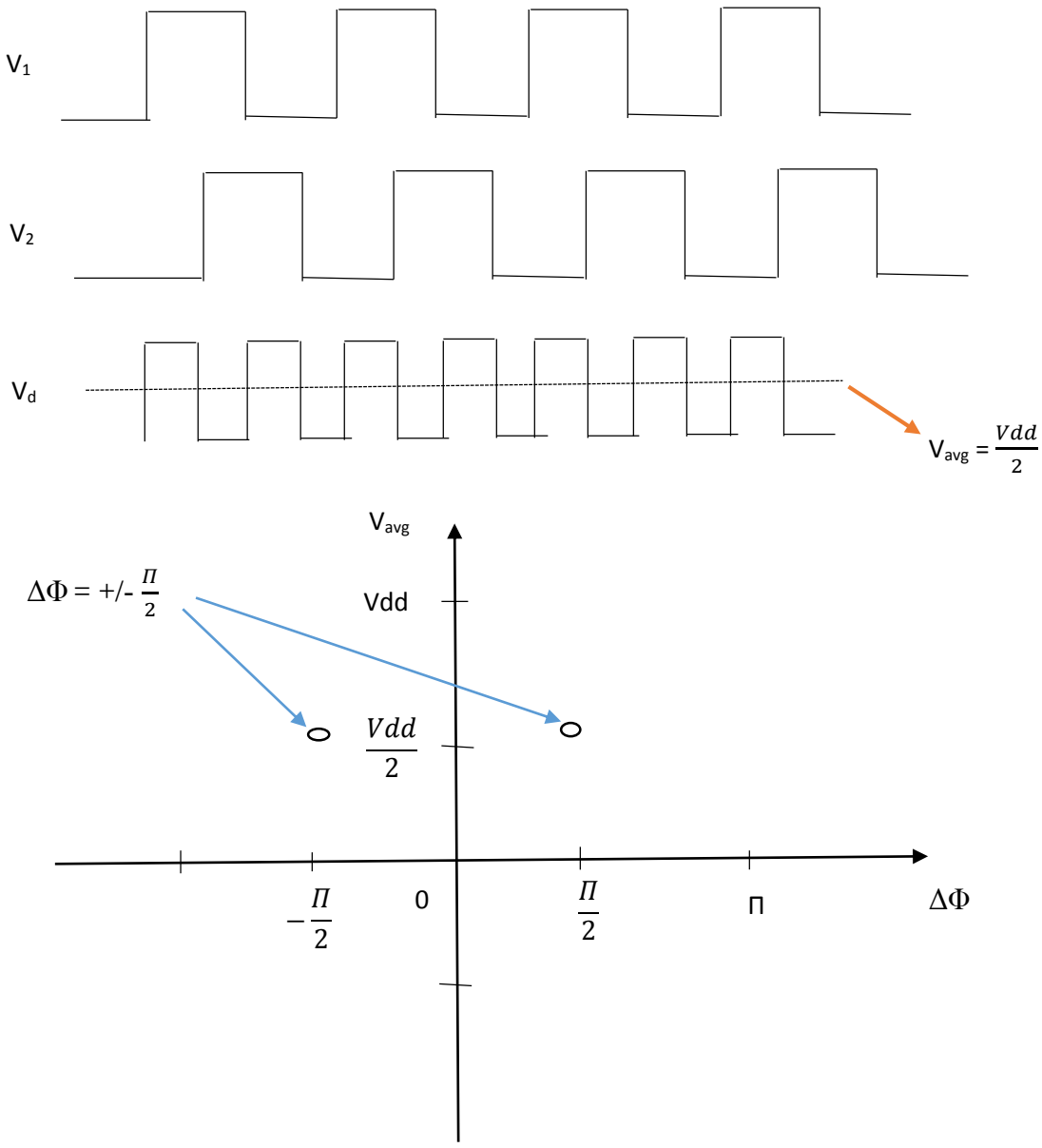



Fig 2.4. EXOR phase detector with $\Delta\Phi = \frac{\Pi}{2}$

In that case output error signal is a square wave which is having frequency that is twice the frequency of input signals. This high frequency signal filtered by LPF, we consider only the average value of output error signal.

**(C)**. When $\Delta\Phi = \Pi$, then

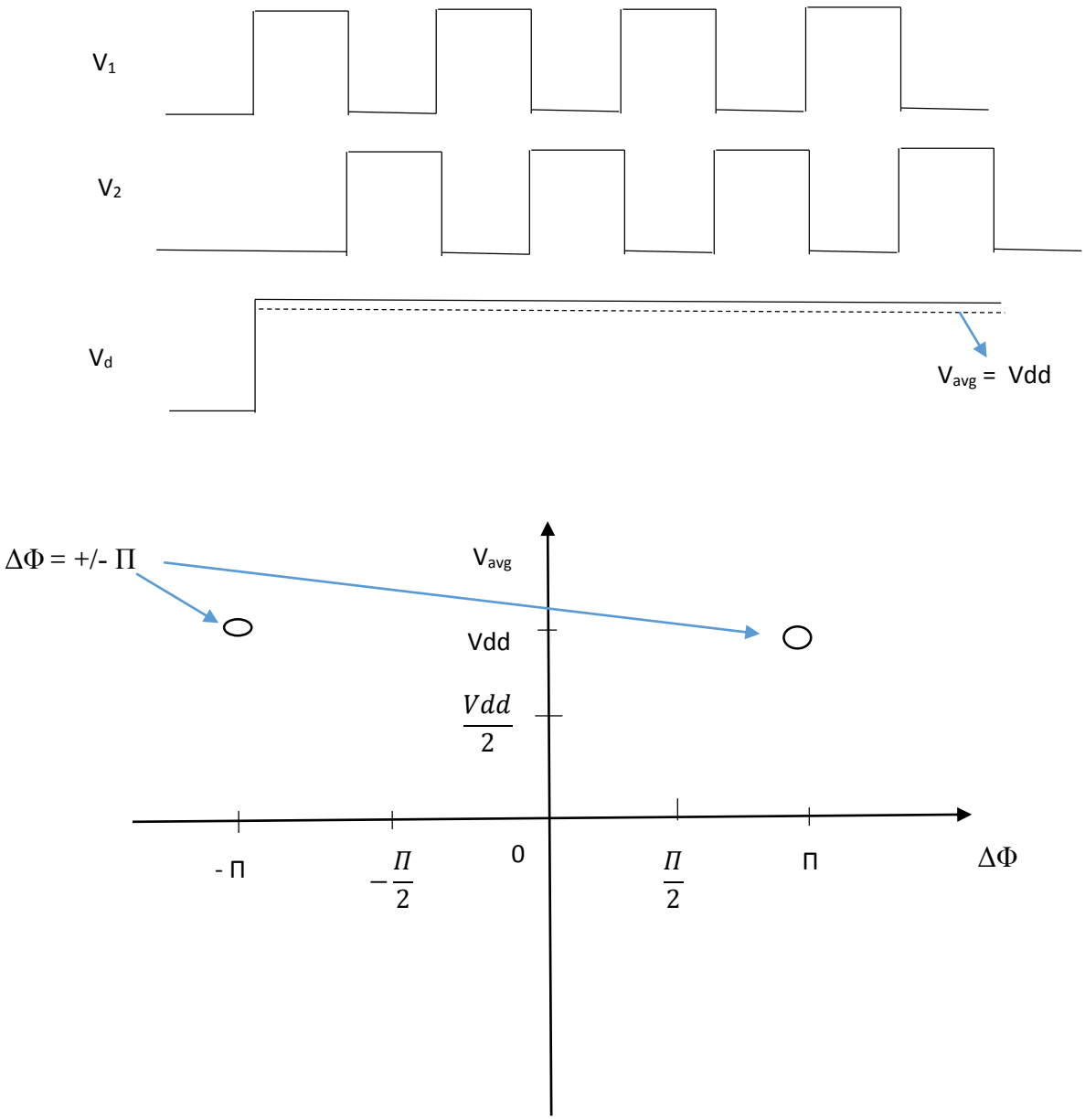



Fig 2.5. EXOR phase detector for $\Delta\Phi = \Pi$

When DPLL is unlocked, then input frequency and feedback frequency are different.

So output error signal of PD contain AC term whose frequency is difference of input signal frequency and feedback signal frequency, harmonics of which filtered by LPF. So we can say that EXOR PD work very similar to the multiplier PD.

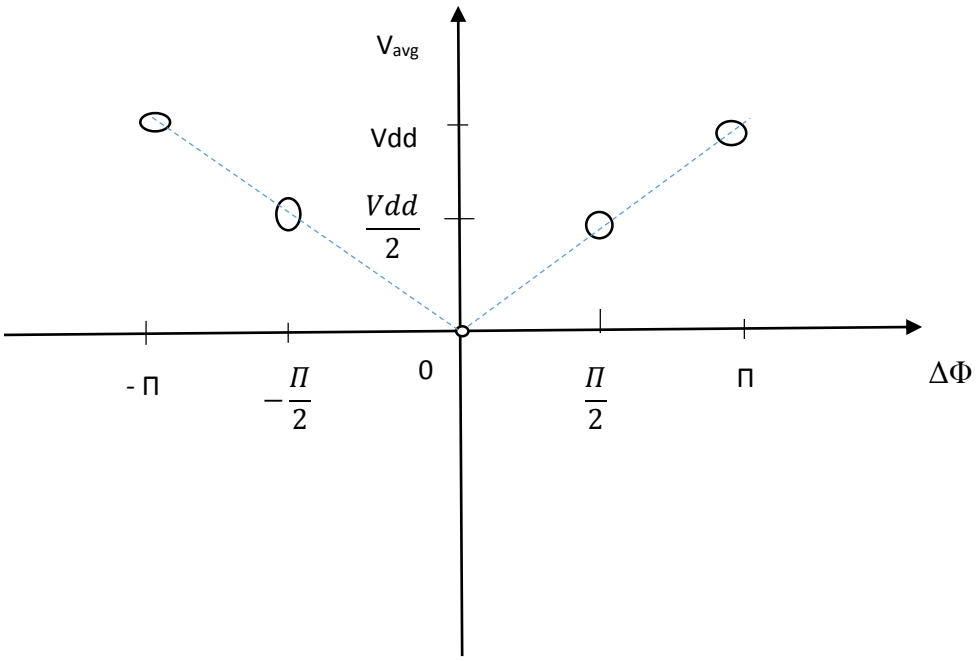



Fig 2.6. PD Characteristics graph of ΔΦ ranging zero to Π

## 3. JK-flip flop phase detector

In JK- flip flop phase detector, JK flip flop different from conventional JK flip flop because that is edge triggered. When positive raising edge appear at J input triggers the output of flip flop into its high state. If positive raising edge appear at K input triggers the output of flip flop into its low state. JK- flip flop phase detectors are used mostly in digital PLL (DPLL). DPLL sense the phase difference between phase's of input signals and generate the output error signal which has liner relation with phase difference (ΔΦ) of input signals. The signals in DPLL are binary signal. We analysis this phase detector for different values of ΔΦ.

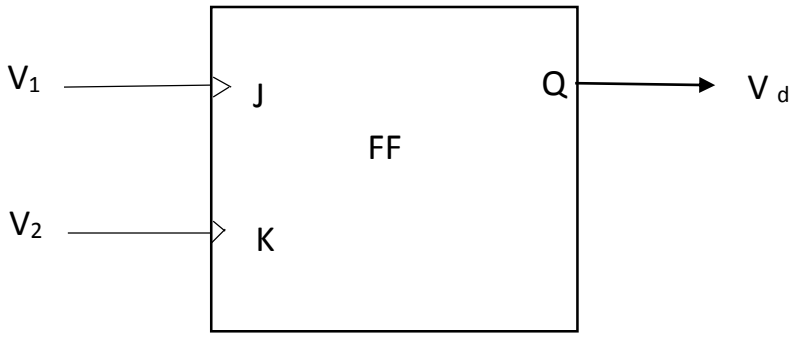



Fig 2.7. JK-flip flop phase detector

**(A).** when $\Delta\Phi = 0$ , then

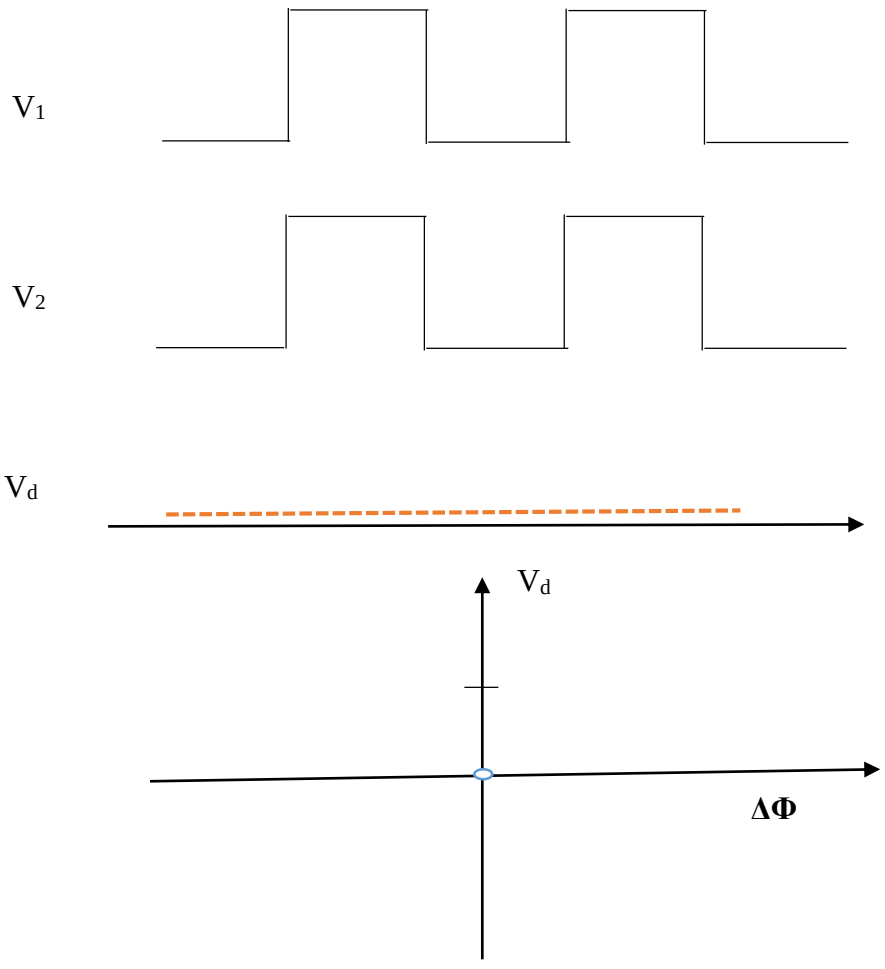



**Fig 2.8. J-K Flip flop phase detector with $\Delta\Phi = 0$**

**(B)**. When $\Delta\Phi = +/- \frac{\Pi}{2}$ , then

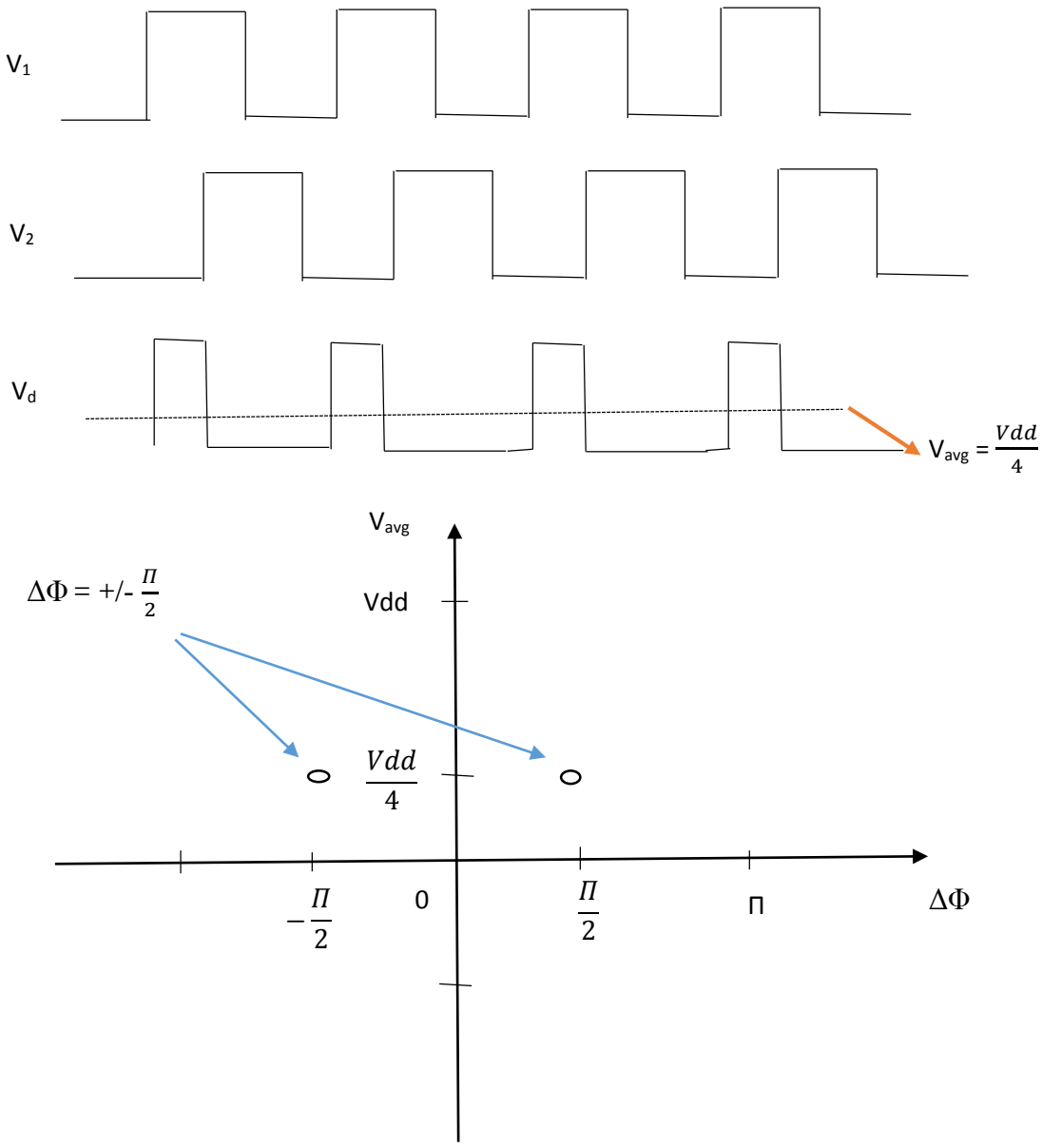



**Fig 2.9.JK-flip flop phase detector with $\Delta\Phi = +/- \frac{\Pi}{2}$**

In that case output error signal is a square wave which is having frequency that is same the frequency of input signals. This high frequency signal filtered by LPF, we consider only the average value of output error signal.

**(C)**. when $\Delta\Phi = \Pi$, then

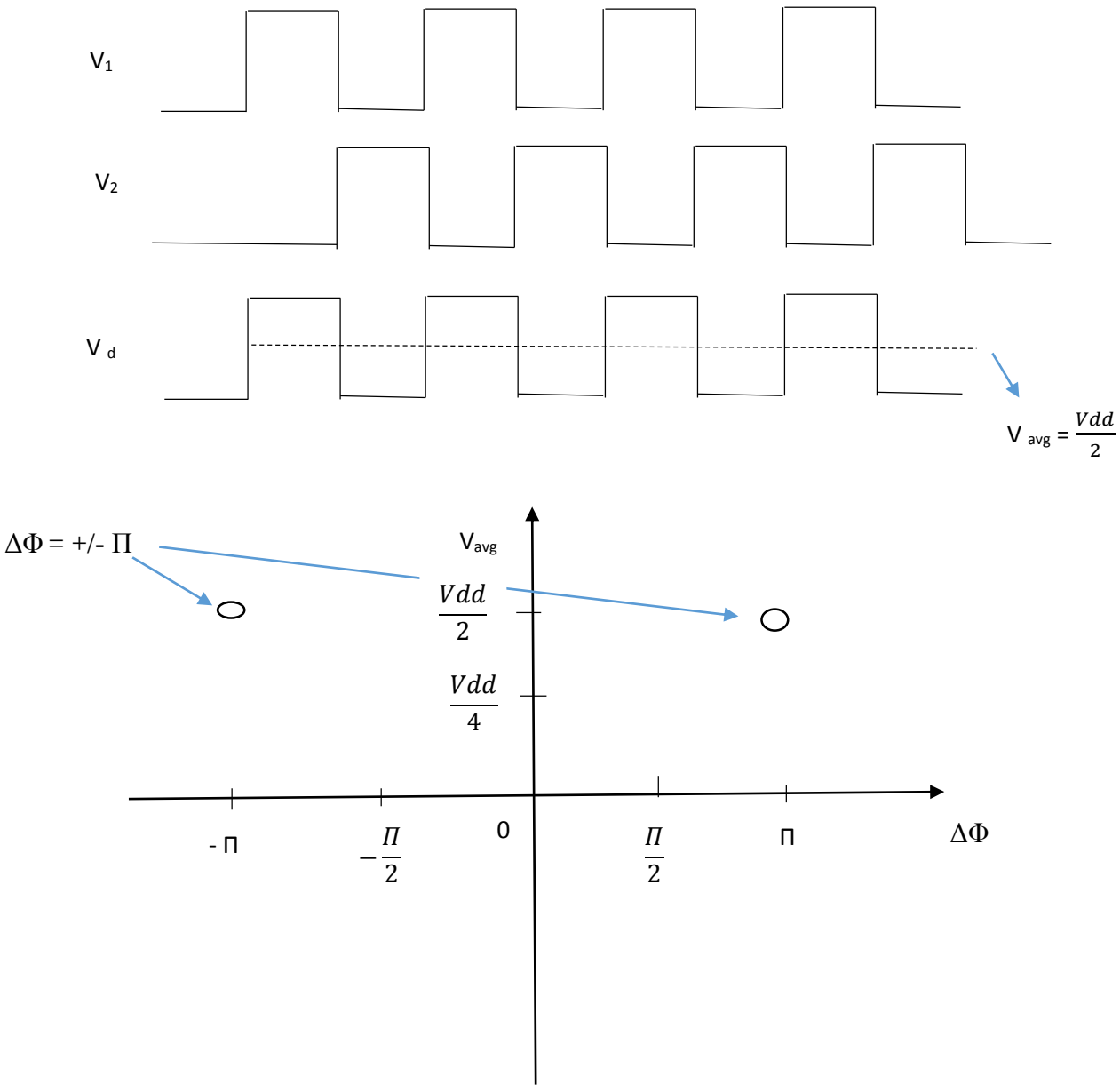



**Fig 2.10. EXOR phase detector for ΔΦ = Π**

When DPLL is unlocked, then input frequency and feedback frequency are different.

So output error signal of PD contain AC term whose frequency is difference of input signal frequency and feedback signal frequency, harmonics of which filtered by LPF. So we can say that JK flip flop PD work very similar to the EXOR PD and multiplier PD.

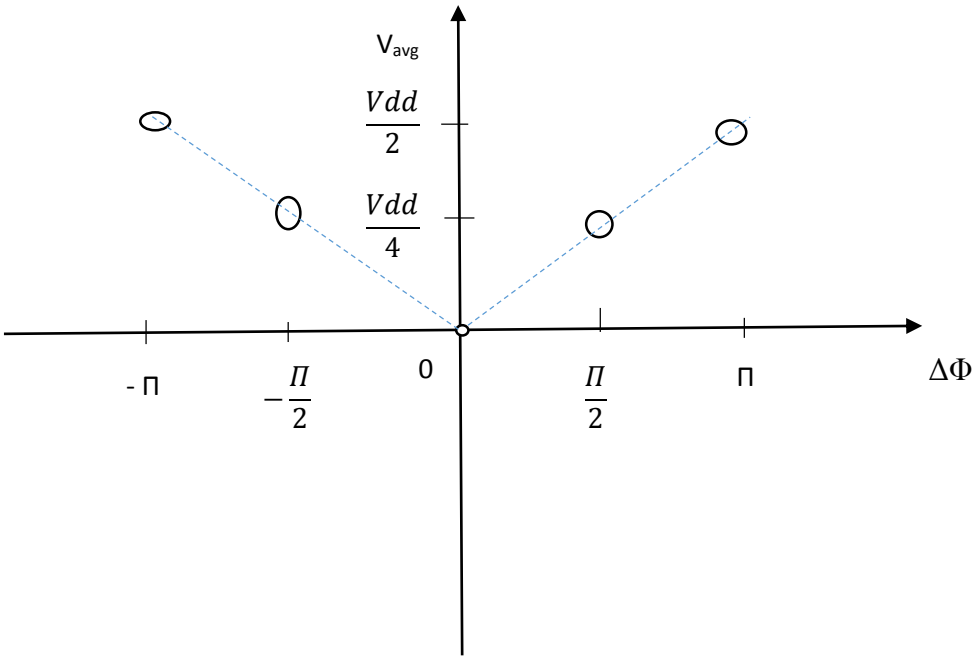



**Fig 2.11. JK-flip flop PD Characteristics graph of ΔΦ ranging zero to Π**

The three different type of phase frequency detector (PD) implemented and analysed here. They have major disadvantage that, they can lock only harmonics of input signal frequency and they cannot detect the difference between input signal frequency and feedback signal frequency.

To take care of this disadvantage, we implement the phase frequency detector (PFD).

## 4. Phase frequency detector (PDF)

PFD can measure the difference in frequency and phase of input signal and feedback signal. So we can say that output error signal does not depend on phase difference also frequency difference between input signal and feedback signal.

The phase frequency detector having two D flip flop with reset signal, whose outputs are UP and DOWN signals. Then these signals are applied to charge pump. PFD also respond to only positive raising edge of the two inputs. The inputs to the clocks of two D flip flop are input signal and feedback signal and the D input connect to Vdd. Then their outputs are UP signal and DOWN signal, these connect to AND to reset the D flip flop. When UP and DOWN signal are high at a time then out of AND is high which reset the D flip flop. So we can say that output error signal UP and DOWN cannot high at the same time. Mean, output error signal may be UP signal or may be DOWN signal but not both.

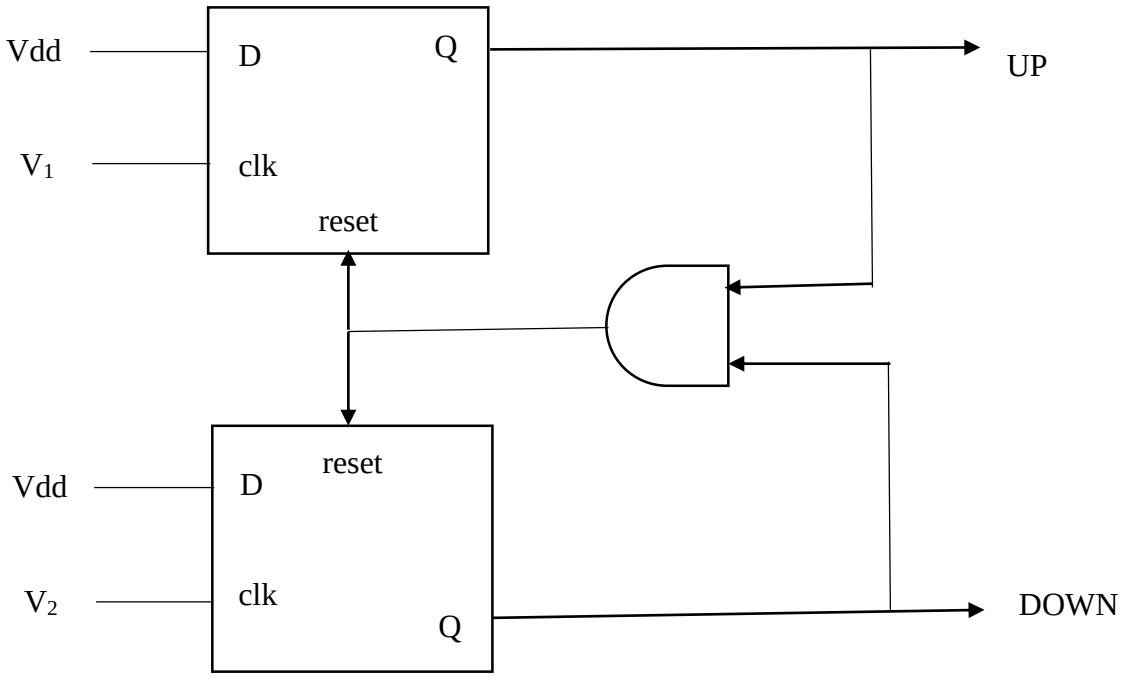



**Fig 2. 12 Block Diagram PFD [2]**

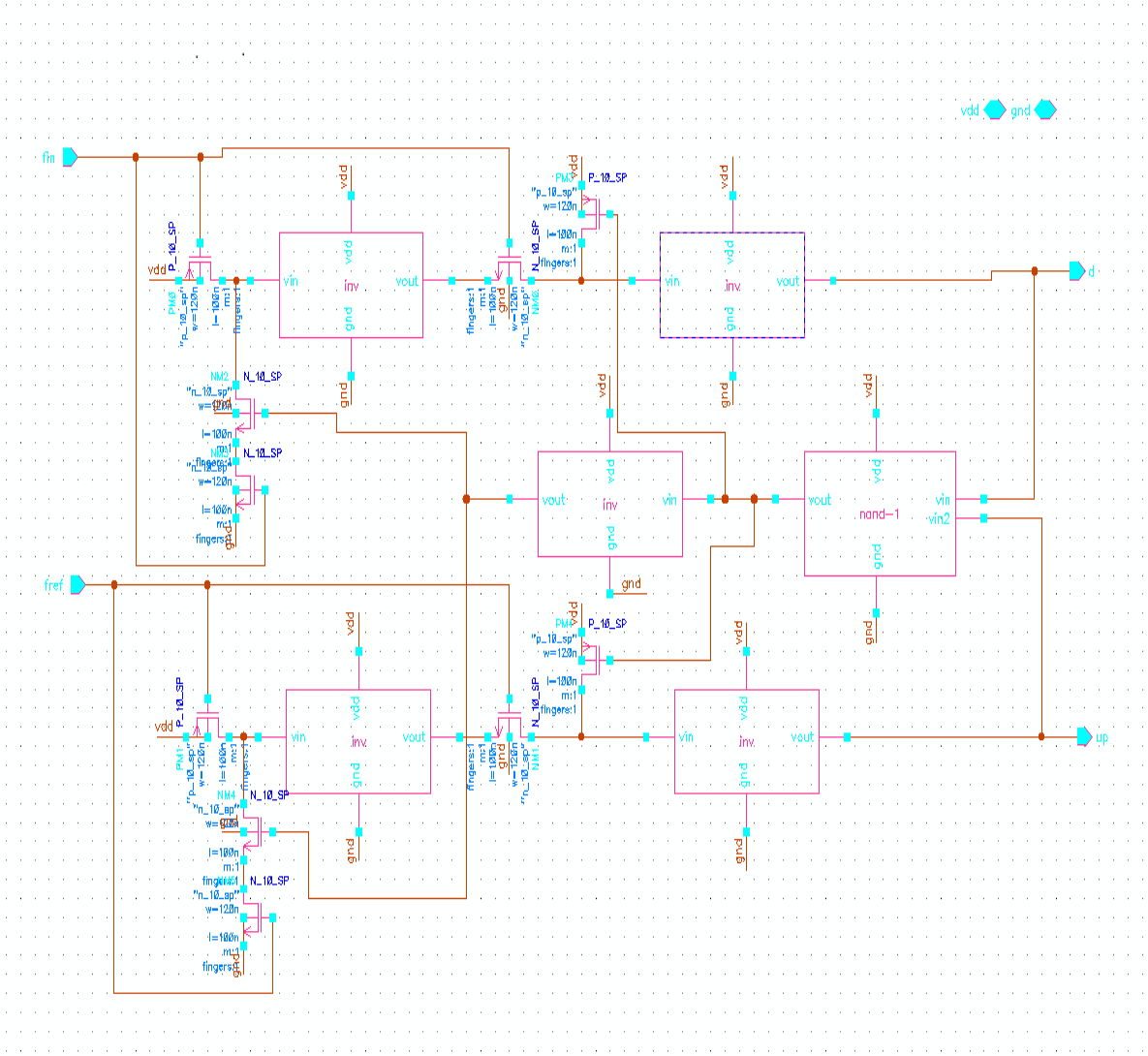



**Fig 2. 13. PFD Implementation [4]**

This PFD circuit analysed in two way, one in which $f_{in}$ leads the $f_{ref}$ and in other in which $f_{ref}$ Leads the $f_{in}$.

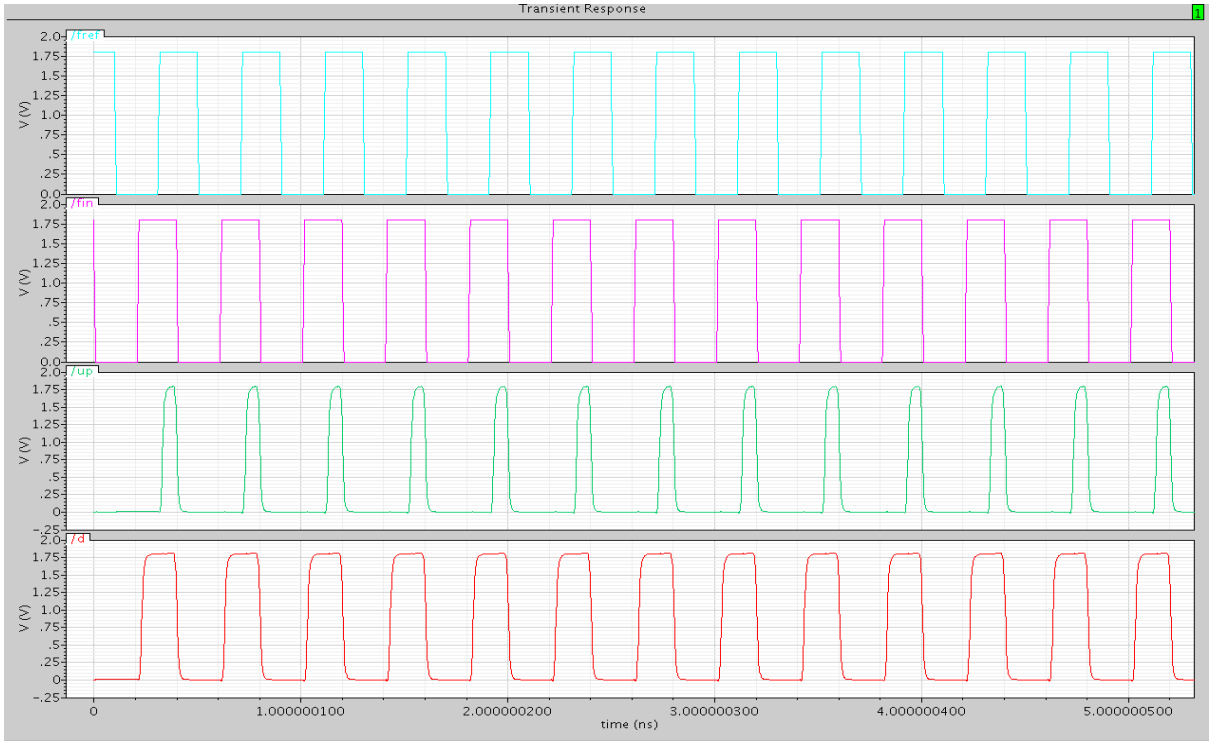



**Fig 2.14. PFD Simulation (fin leads fref)**


**Fig2.15. PFD Simulation (fref leads fin )**

# CHAPTER 3

# CHARGE PUMP

## 3.1 Introduction

The outputs signal of PFD are UP and DOWN which applied to charge pump, which convert the two input to single output. Which increase/ decrease the charge across the capacitor of LPF.

When UP signal is high then PMOS terns on and current flow from power supply to capacitor of LPF by which capacitor of LPF charge to a voltage ($V_{con}$). When DOWN signal is high then NMOS terns on and current flow from capacitor of LPF to ground, by which capacitor of LPF discharge. When both signals are low then both MOSFET are off and output is in high impedance state. The main problem with it is that when UP signal is high then PMOS terns on, if there is a variation in power supply that effect the voltage across the capacitor of LPF.

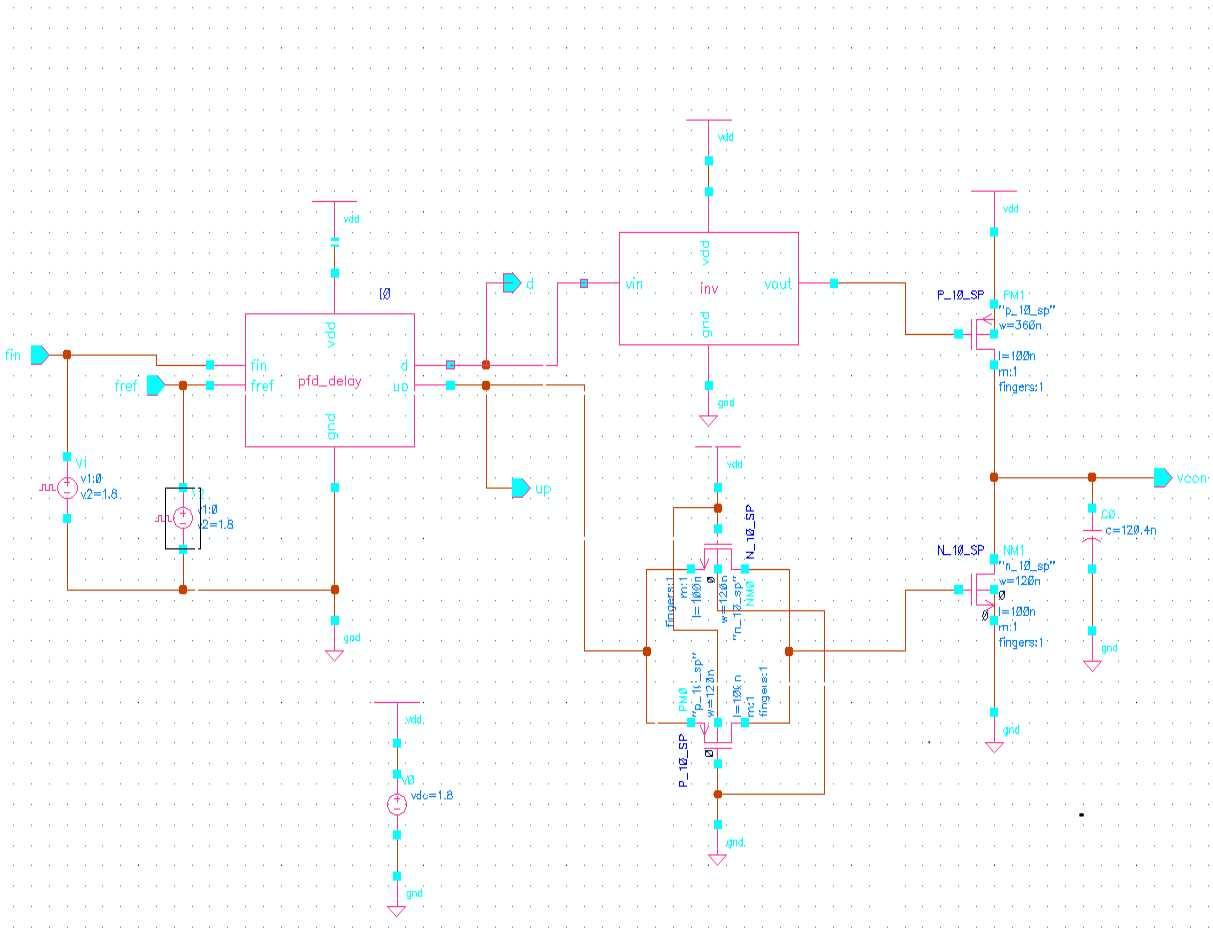



**Fig 3.1. Tri-state schematic**

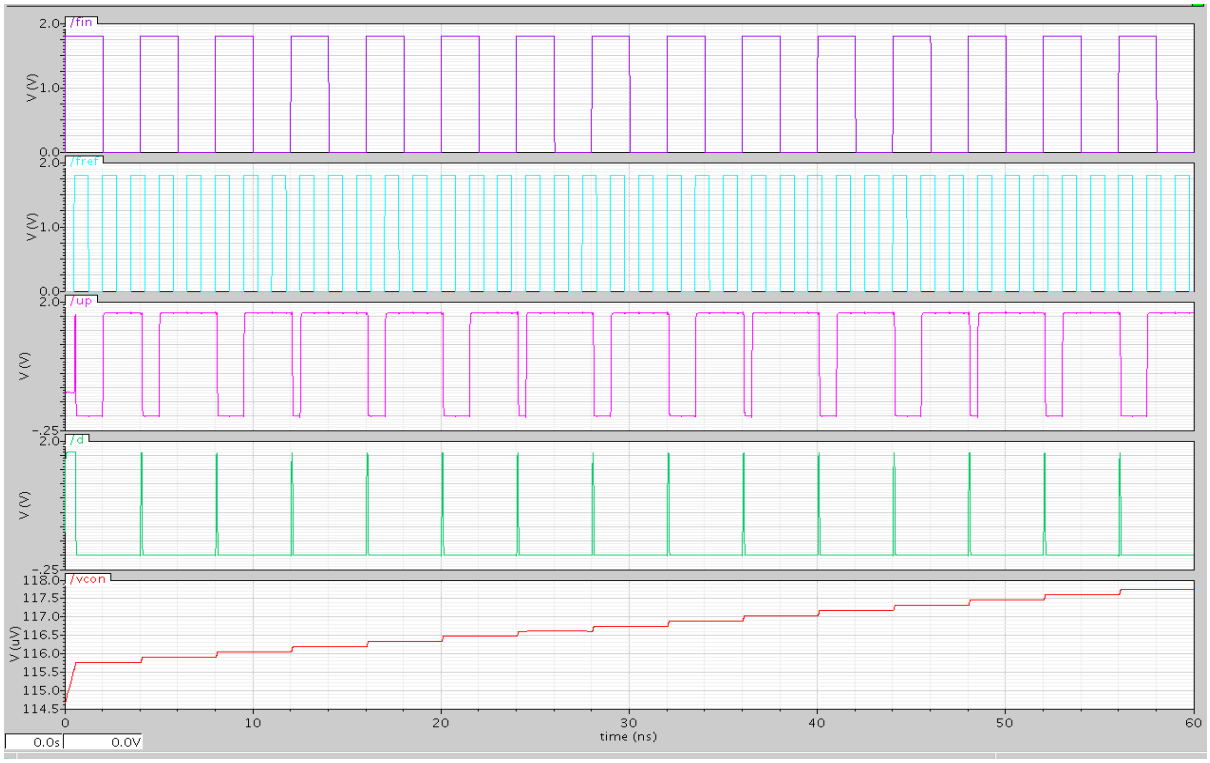



**Fig 3.2. Tri-state output Simulation**

Now consider the variation in power supply and find out what is the effect on voltage across the capacitor of LPF.

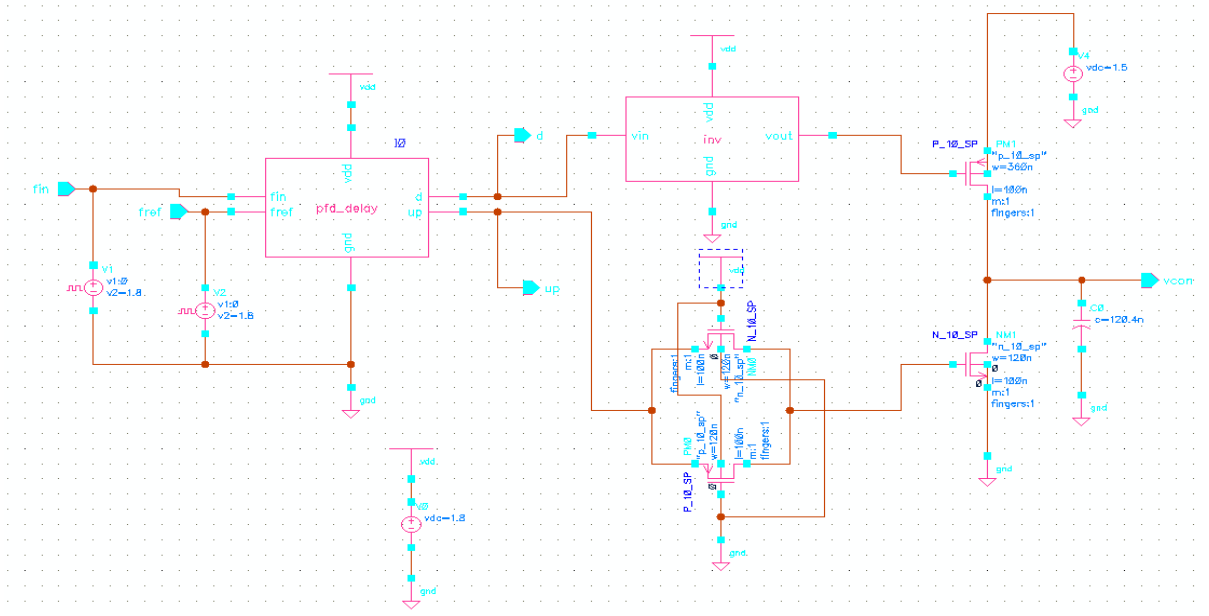



**Fig 3.3. Tri-state Vdd Variation Schematic**

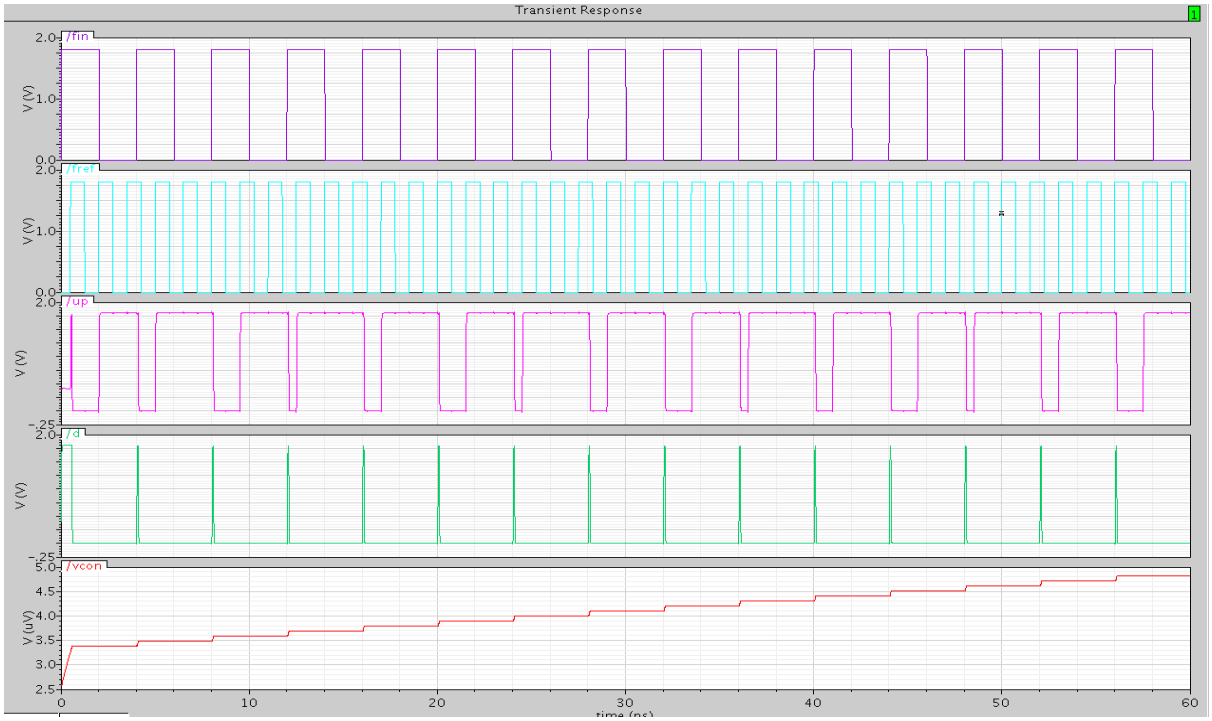



**Fig 3.4. Tri-state Vdd variation Output Simulation**

## 3.2 Modified Charge Pump

To avoid the effect of power supply on the voltage across the capacitor of LPF, we used the two current sources. When UP signal is high then PMOS terns on and charge the capacitor by a current source. If DOWN signal is high then NMOS terns on and discharge the capacitor by a current source. NMOS and PMOS are operated in linear region and act like resistor. They should have large W/L ratio for fast switching. When W/L ratio is large then on resistance should be small. As the on resistance is small then voltage across is also small. So we will get wide voltage swing at output node. There are two current sources which can be implemented by NMOS and PMOS. They consume the overdrive voltage which is limited the voltage swing at output node. In real life, we do not have ideal current sources which having infinite resistance. So there will be small error as we used NMOS and PMOS as current sources.

To adjust the delay between UP signal and DOWN signal, we can use the complimentary pass gate between DOWN and NMOS.

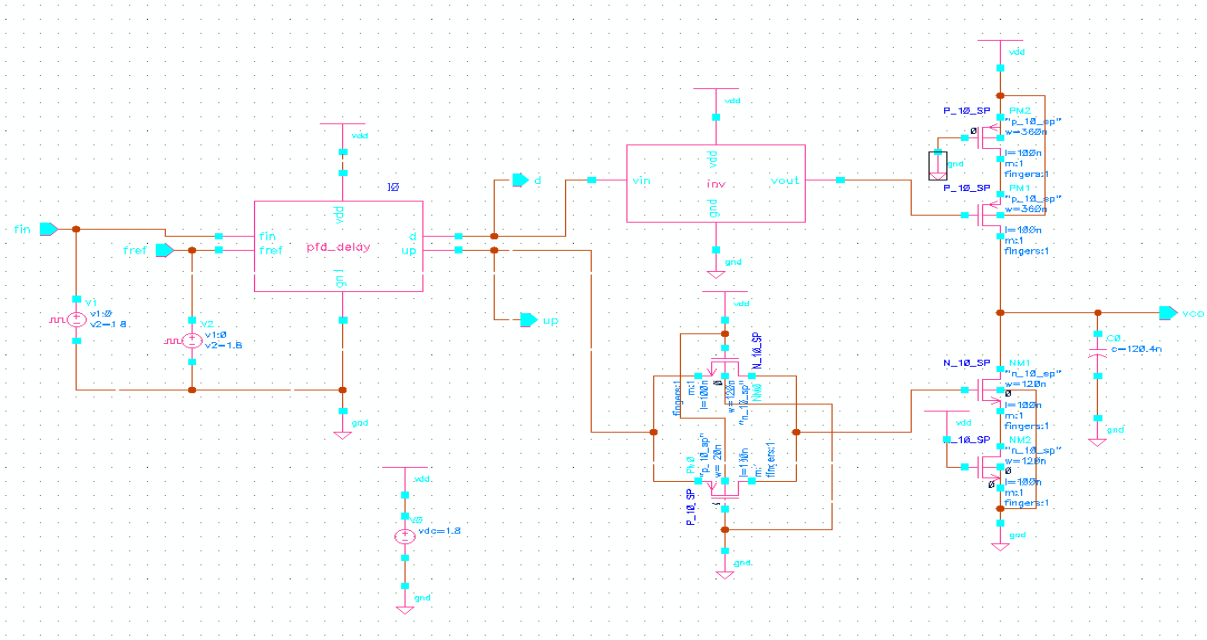



**Fig 3.5. Schematic of Modified Charge Pump**

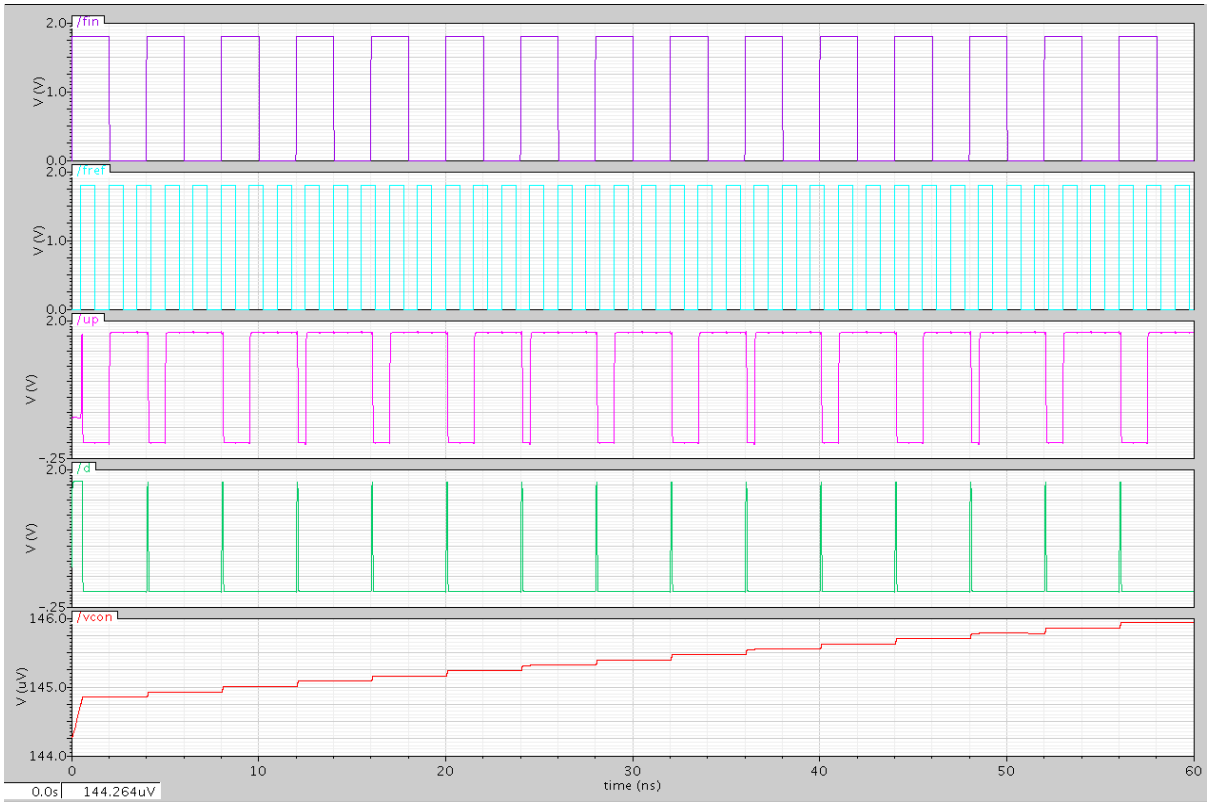



**Fig 3.6. Modified Charge Pump Simulation**

In section, I describe the effect of power supply on the voltage across the capacitor and conclude that modified charge pump less effect by supply voltage when it compare with tri-state configuration. So we can say that, this modified charge pump can be used in the PLL.

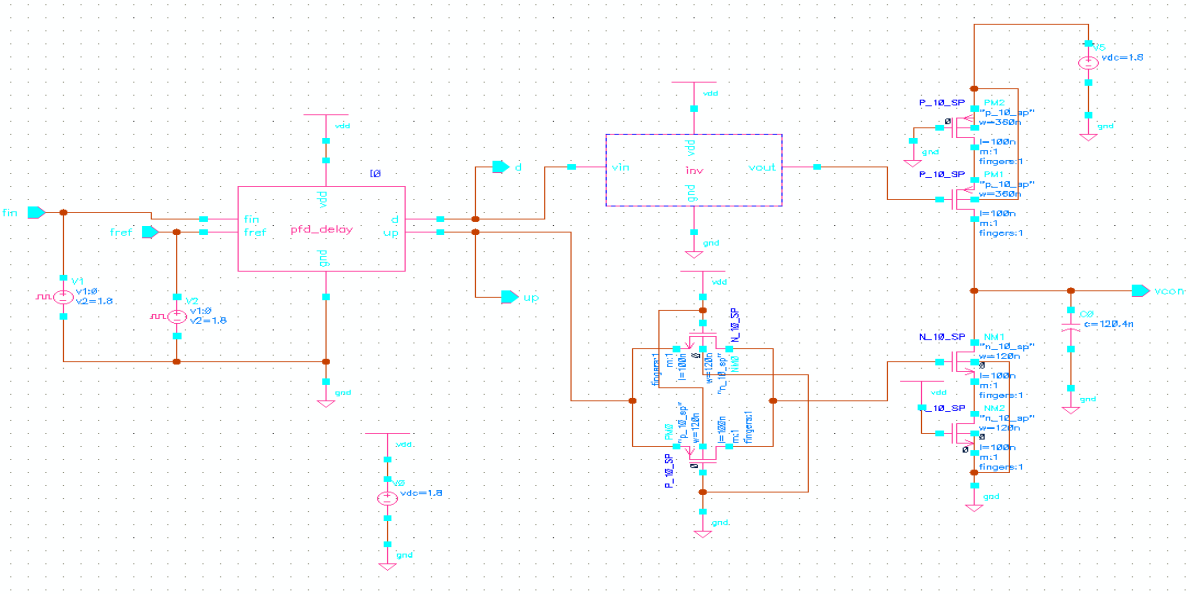



**Fig 3.7. Schematic of Modified Charge Pump with Vdd Variation**

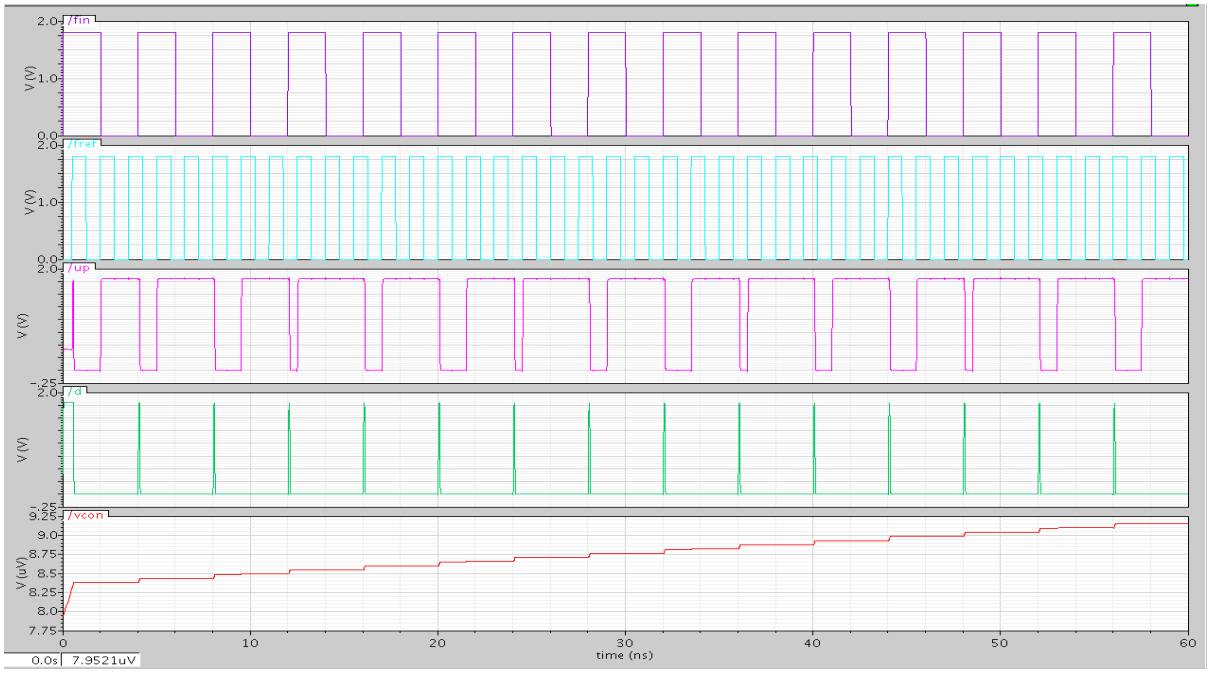



**Fig 3.8. Simulation of Modified Charge Pump with Vdd Variation**

# CHAPTER 4

# LOOP FILTER

## 4.1 INTRODUCTION

Why, we used loop filter in PLL. If consider the PLL without loop filter. The error output signal from PFD direct applied to VCO which modulate the frequency of VCO but output error signal contain dc term and high frequency term. The high frequency term is undesirable because input to the VCO should be dc voltage.so to remove that ac term we used a capacitor which stop the all high frequency signals. Now we can say that loop filter is main component of PLL.

## 4.2 Transfer Function of PLL

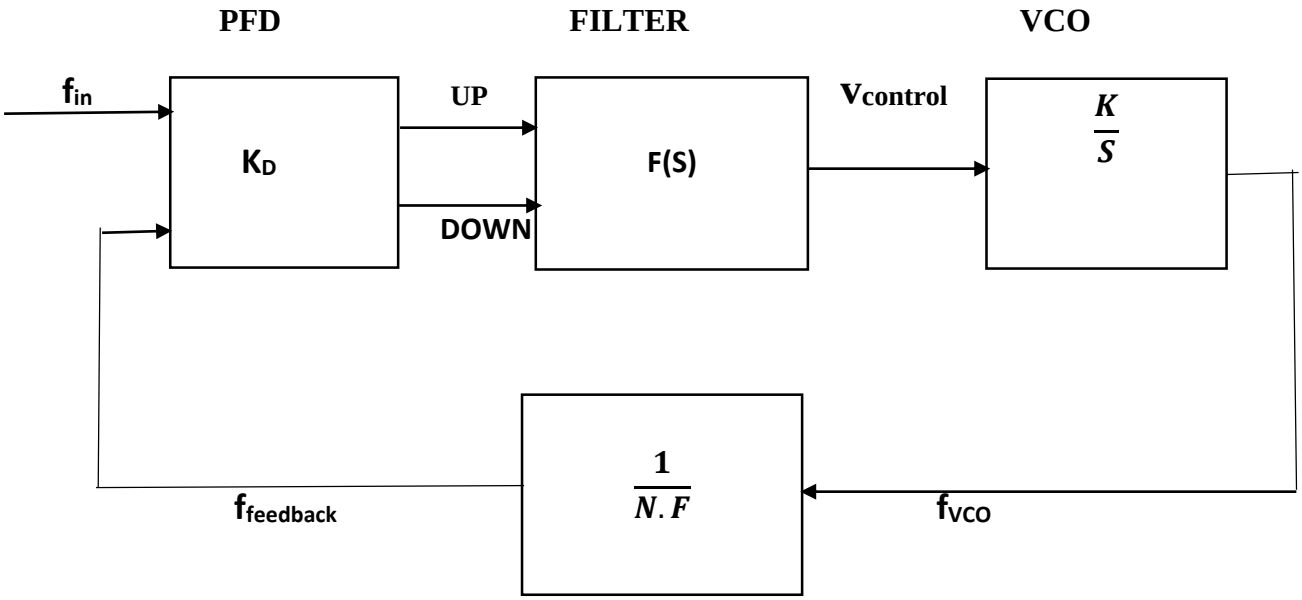



**Fig 4.1. Mathematical model of PLL [1]**

Now consider that loop filter having only capacitor then

$$F(S) = \frac{1}{C.S} \qquad \ldots\ldots\ldots\ldots 1$$

The open loop transfer function for forward path is given as

$$G(S) = K_D.\frac{1}{C.S}.\frac{K}{S} \qquad \ldots\ldots\ldots\ldots\ldots 2$$

Now closed loop transfer function of PLL is given as

$$T(S) = \frac{KD.\frac{1}{C}.K}{S^2 + \frac{KD.\frac{1}{C}.K}{N.F}} \qquad \text{……..3}$$

From eq .(3) , we can say that closed loop contains two imaginary pole. By which we can say that, closed loop system is unstable. The instability generated because open loop system having pole at zero and each pole provide the constant $90^0$ phase shift [1].

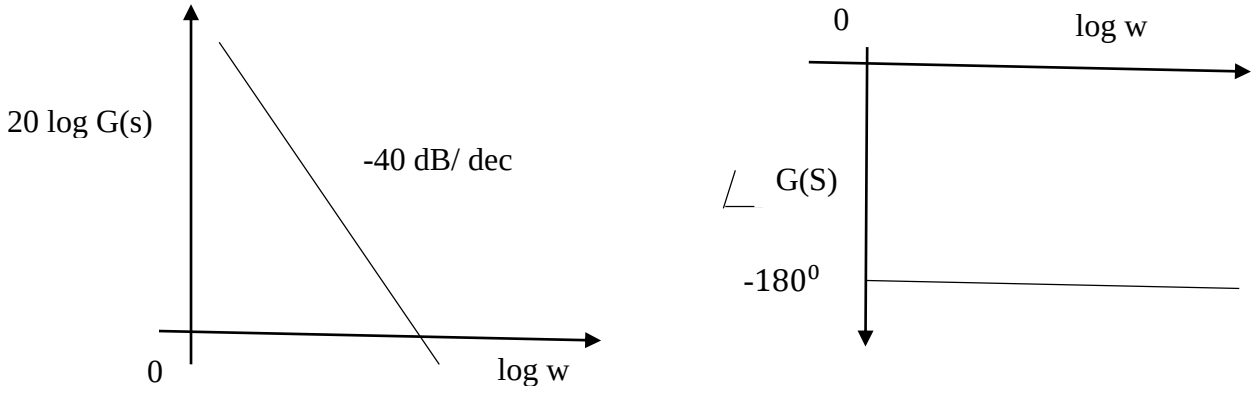



**Fig 4.2. Open loop characteristics [1]**

In order to stabilize the closed loop system, we must modified the phase characteristics such that the phase shift less than $180^0$ at the gain cross over frequency. This is possible by adding an zero in the open loop transfer function. So we can add resistor in series with capacitor of loop filter. Now

$$F(S) = \frac{1}{C.S} + R \qquad \text{……4}$$

The open loop transfer function for forward path is given as

$$G(S) = K_D.(\frac{1}{C.S} + R).\frac{K}{S} \qquad \text{…….5}$$

Now closed loop transfer function of PLL is given as

$$T(S) = \frac{KD.k.(1+RCS)}{S^2 + \frac{KD.K.R.S}{N.F} + \frac{KD.K}{N.F}} \qquad \text{.....6}$$

Now, the closed loop transfer function of PLL contain an zero at $S_z = -1/RC$.

By using eq. (6):

$$W_n = \sqrt{\frac{KD.K}{N.F}} \quad \text{and} \quad \zeta = \frac{C.R}{2}.\sqrt{\frac{KD.K}{N.F}} \qquad \text{.....7}$$

$W_n$ is natural frequency and $\zeta$ is damping ratio.

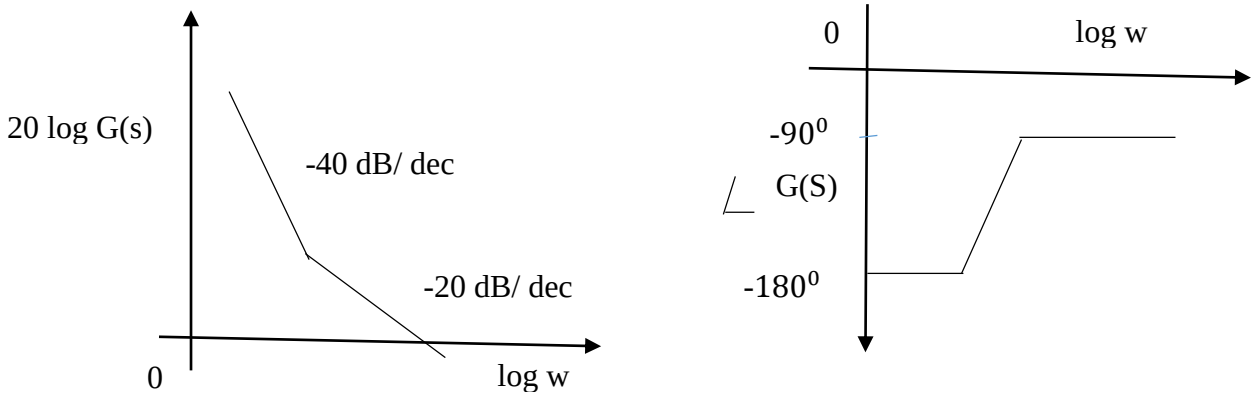



**Fig 4.3. Open loop characteristics with addition of zero [1]**

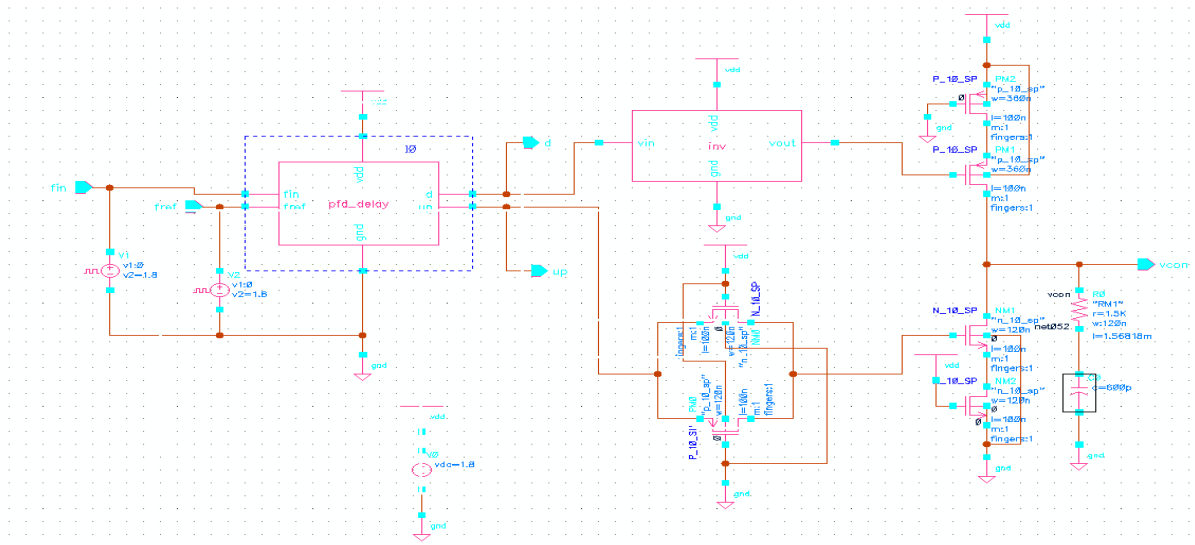



**Fig 4.4. Schematic of PFD, CP and filter with R and C**

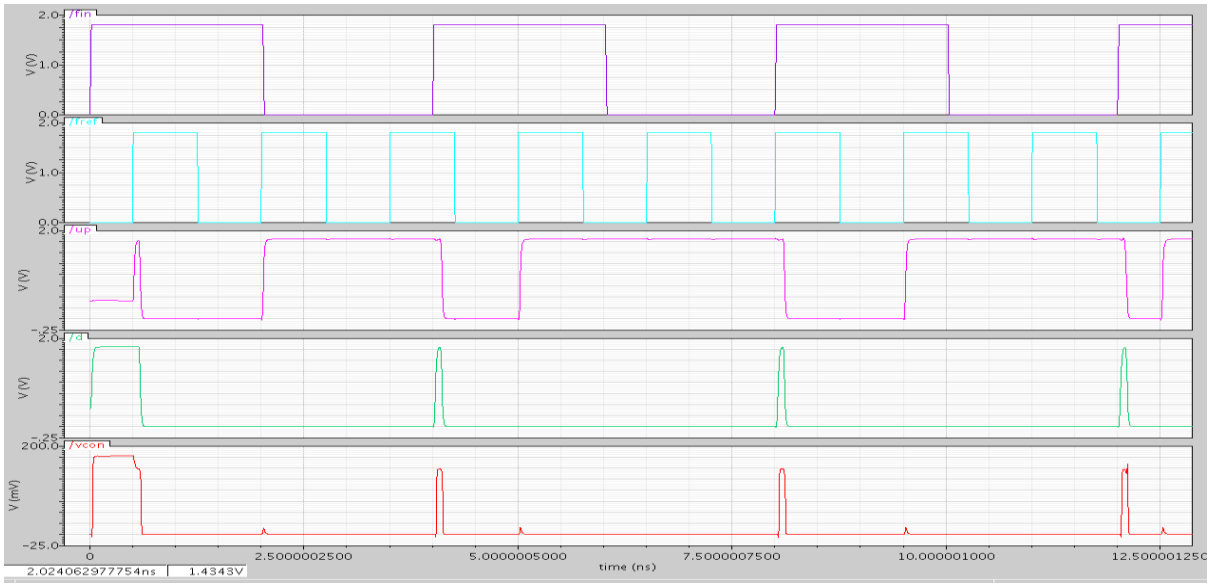



**Fig 4.5. Simulation of PFD, CP and filter with R and C**

The modified PLL having another problem. Since the charge pump drives the series combination of R and C of loop filter, each time a current flow through the R and C of loop filter so control voltage experiences the large jump. Which effect the performance of VCO. To avoid this, another capacitor ($C_1$) added parallel with R.

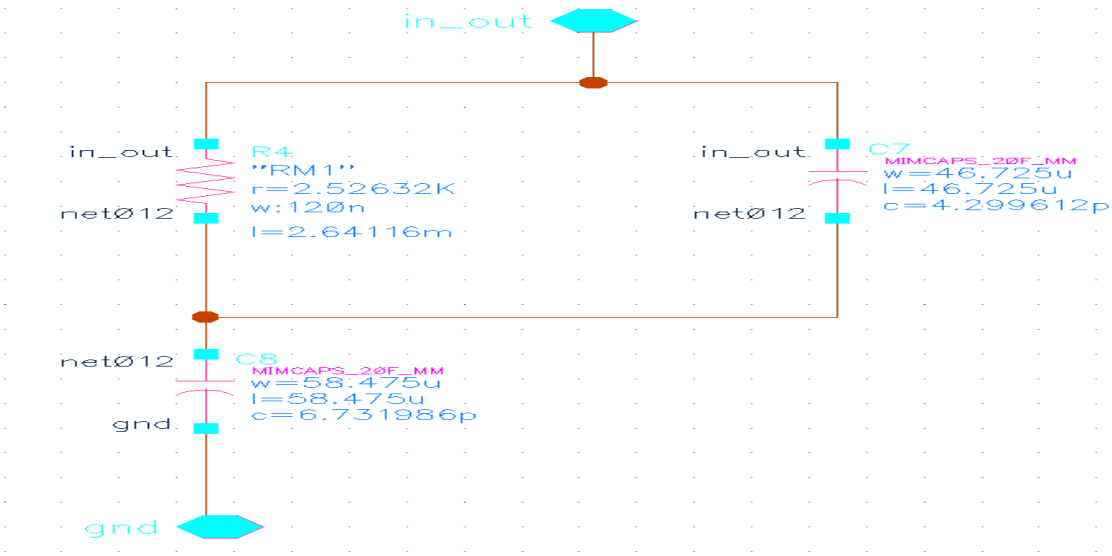



**Fig 4.6. Schematic of loop filter with R, C and $C_1$**

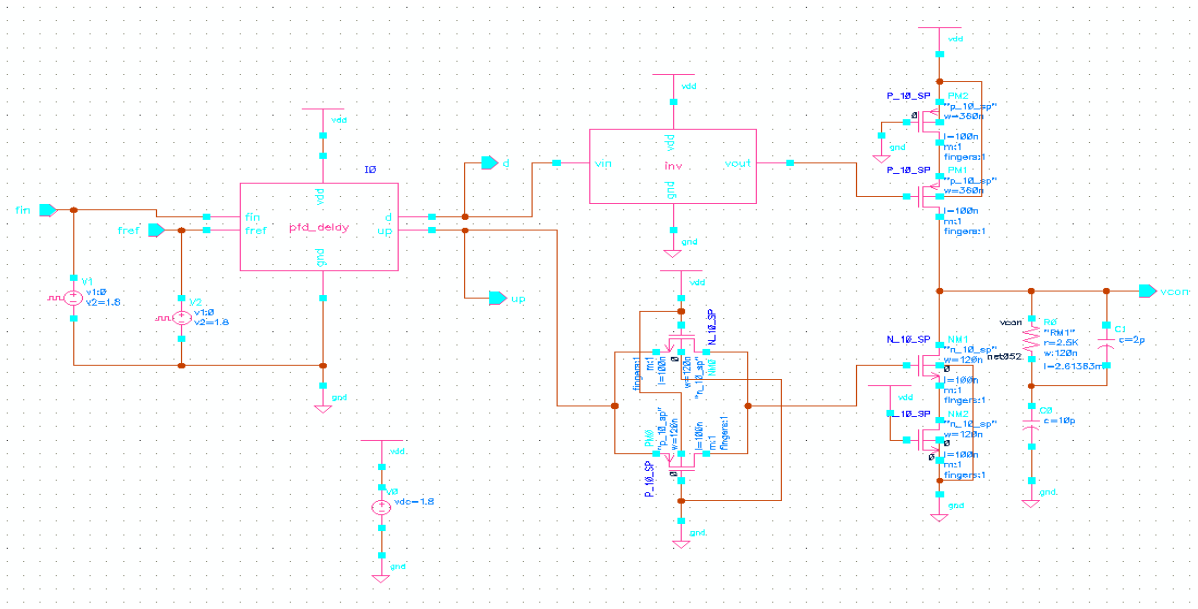



**Fig 4.7. Schematic of PFD, CP and filter with R, C and $C_1$**

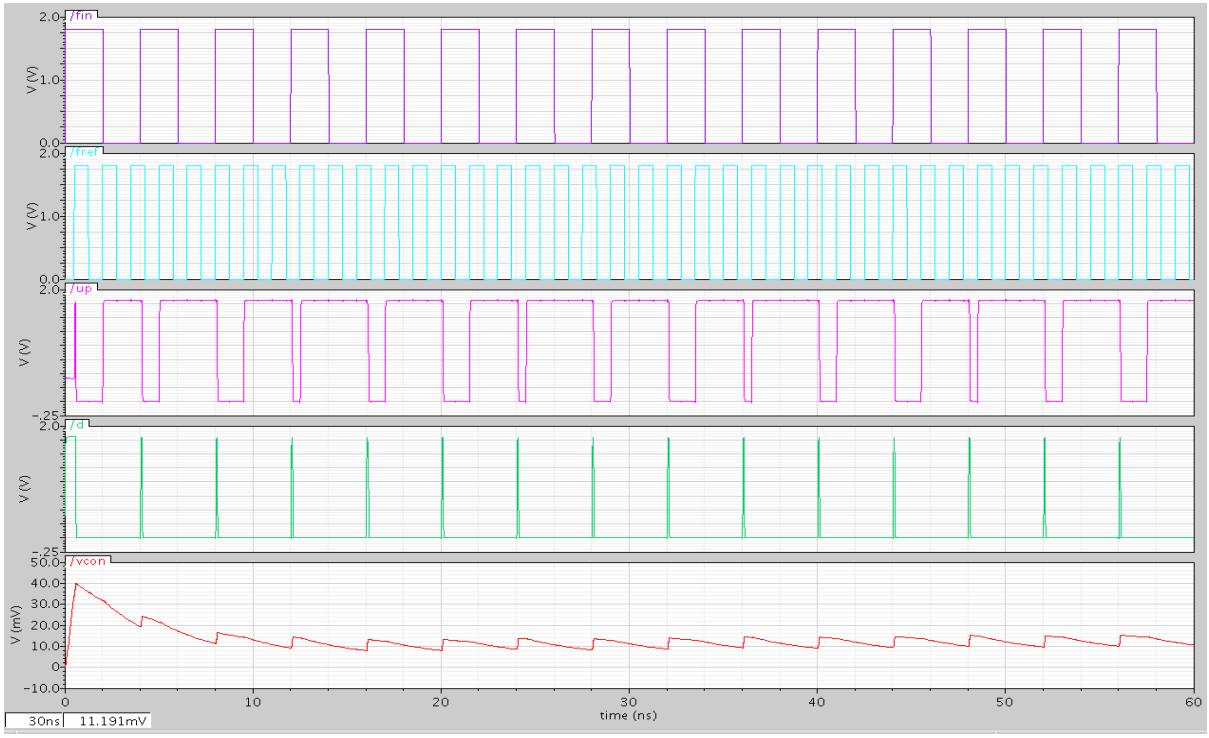



**Fig 4.8. Simulation of PFD, CP and filter with R, C and $C_1$**

# CHAPTER 5

# VOLTAGE CONTROLED OSCILATOR

# 5.1 INTRODUCTION

An oscillator is a circuit that generate a periodic signal without any input signal. Now, consider the unity gain negative feedback system.

$$\frac{Vout}{Vin} = \frac{T(S)}{1+T(S)}$$

This circuit may oscillate at $W_o$ if satisfy the " Barkhausen criteria ". These condition are necessary but not sufficient. These condition given as

1. $\left|T(jW_o)\right| = 1$
2. Angle $\{T(jW_o)\} = 180^0$

As T(S) = -1, then gain of the circuit become infinite, which result in infinite amplification of noise component at the oscillation frequency. These criteria means that returning signal is a negative replica of input signal. Which will give the an large difference between input signal and feedback signal when subtracting. The circuit is said to the regenerate. At some point the amplitude of regenerating feedback system will be the limited and barkhausen criteria of a feedback system gain = 1, is fulfilled and gives the a stable oscillation.

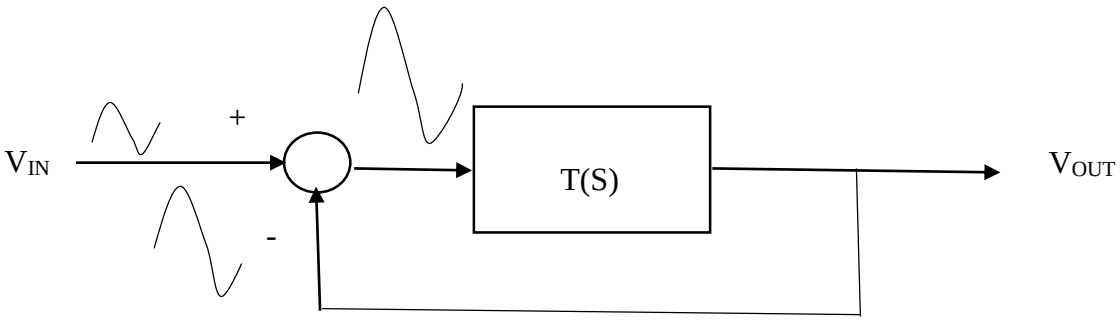



**Fig 5.1. Regenerating Feedback System**

The ring oscillator show in the fig. (5.2), which have odd number of inverter and output frequency of ring oscillator is controlled by supply of inverters. The slope of frequency versus the control signal curve at oscillation frequency is called the voltage-to-frequency (or current to- frequency) conversion gain. Ideally, for linear analysis to apply over the large frequency range. Voltage gain of the VCO needs to be relative constant, The purpose of VCO is to vary the an output frequency proportional to control voltage input.

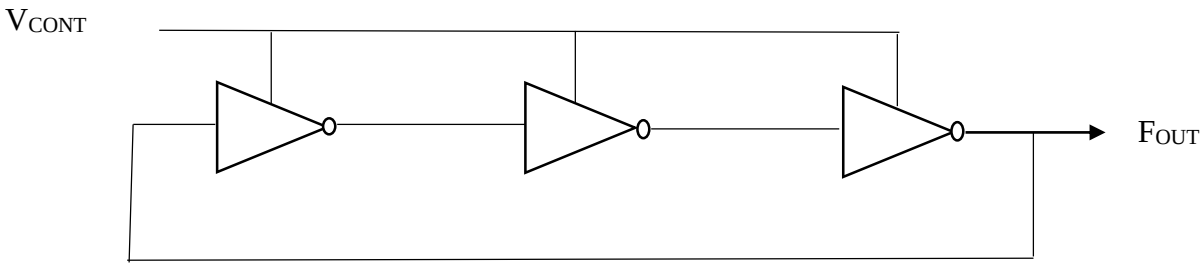



**Fig 5.2. Five Stage Ring Oscillator**

There are two types of VCO architectures can be used in this design. The first is a single-ended ring oscillator, as shown in Fig 5.2 . This design can be used only an odd number of inverters.

$$F_{out} = \frac{1}{2.N.\tau delay}$$

As the equation, we can say that the output frequency of this configuration is proportional to number of stage and the delay of each block. The ring oscillator design in this configuration is very simple but it has some disadvantage. First, it used only an odd number the inverters in order for circuit to not latch up and the another main difficulty is using ring oscillators in wireless communication systems, which has their poor phase noise response.

Because of these disadvantage, we used the differential ring oscillator. The main reason for use the differential ring oscillator is, it offer the better noise rejection.

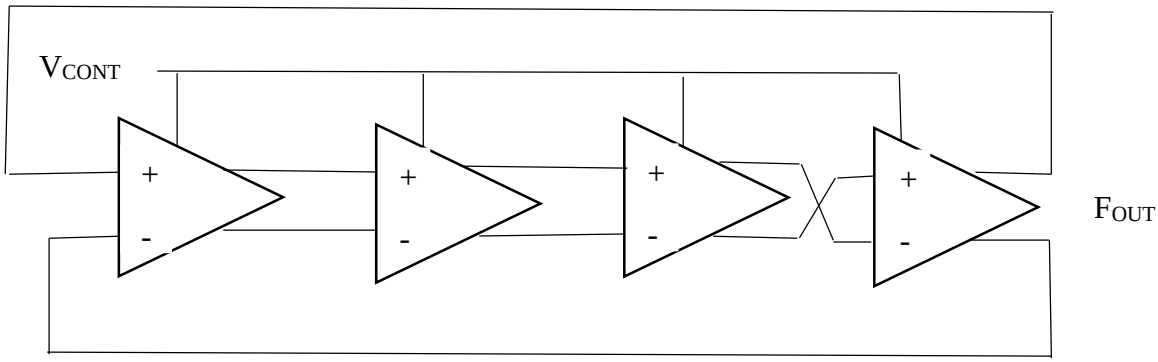



**Fig 5.3. Differential Ring Oscillator**

As shown in the figure, there is inversion between third and fourth stage because of even number of the stages are used. But oscillation frequency of this configuration is same as the single ended configuration. The difference between these two designs is that, the differential style offer more flexibility compare to single ended style in change the frequency of oscillation because it is not restrict to use of odd number of stage. This is another advantage of this style.

## 5.2. Current Starved VCO

VCO is a circuit which generate the periodic signal that have liner relation with control voltage.

Current starved VCO having PMOS and NMOS in middle which perform like inverter, while upper PMOS and lower NMOS work as current source. Current source limited the current through the inverter. The first NMOS and PMOS mirror the current to each stage of inverter. Since the propagation delay of the inverter stage is proportional to the current of inverter stage which supply to output node. Now we can say that, we can control the output frequency easily.

The oscillation frequency of current starved VCO for 'N' stage is given as

$$F_{out} = \frac{1}{N.Td}$$

The $T_d$ is represent the total time taken by $C_T$ to charge and discharge. Given as

$$T_d = \frac{CT.Vdd}{Id}$$

Where the $C_T$ represent the total capacitance on drain of PMOS and NMOS of inverters. And given as

$$C_T = C_{OX} .(W_P.L_P + W_N.L_N) + \frac{3}{2} . C_{OX} . (W_P.L_P + W_N.L_N)$$

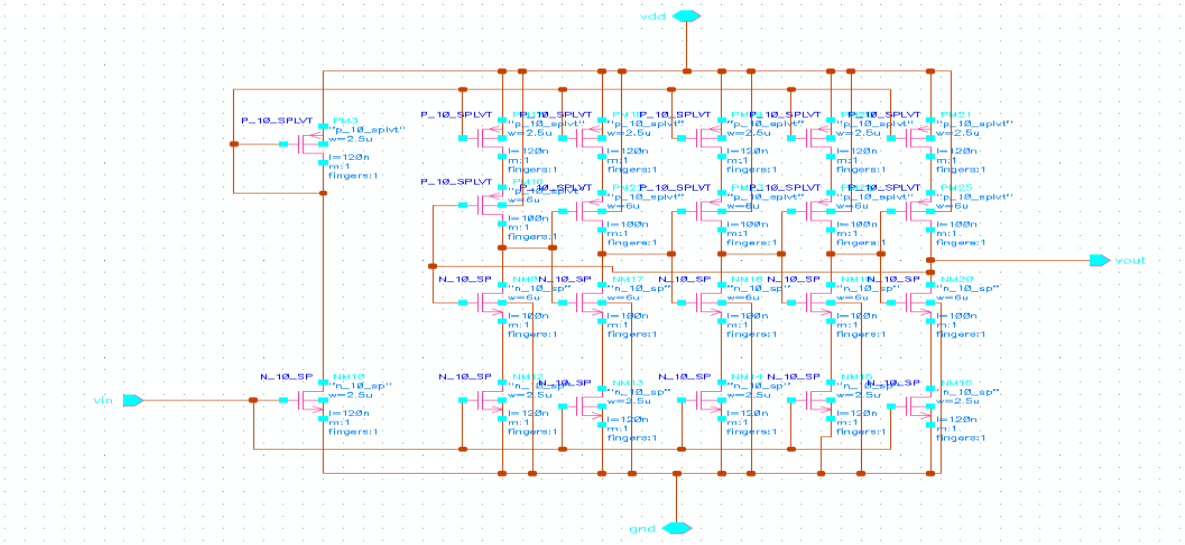



**Fig 5.4. Schematic of Current Starved Ring Oscillator**

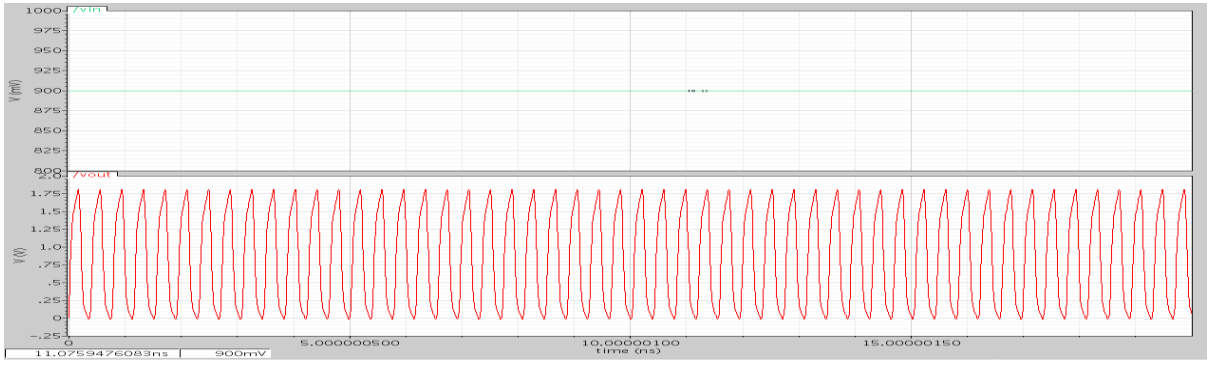



**Fig 5.5. Simulation of Current Starved Ring Oscillator for $V_{cont}$ = 900mv**

# CHAPTER 6

# DIVIDER

## 6.1. INTRODUCTION

In PLL as a frequency synthesizer, we used a divider circuit in feedback path which divide the output frequency of voltage controlled oscillator (VCO) by a number. The divider number may be integer or fractional. Divider circuit is design by many method, but I design by using the double edge trigger flip flop. Which having two normal D flip flop, clk, $\overline{clk}$ and multiplexer.

We also design the AND gate by using "differential cascade voltage switch logic" (DCVSL) which is very fast. DCVSL provide the differential output, so we get the natural inversion; mean a single stage can serves as both NAND and AND gate.

## 6.2 Design of AND gate

A differential circuit must be used to improve noise resistance. There may be increase the transistor count but it improve the noise resistance and it is very fast. Because of the differential output, we will get the both AND and NAND gate. The fast response due to the feedback which provided by two PMOS load. These PMOS load must having small W/L ratio to minimise the parasitic capacitances and maximise the speed. The NMOS also having small W/L ratio because they also drive the capacitor load. By using small W/L ratio of PMOS and NMOS results the reduction of the power consumption. In circuit, when both input is zero then both NMOS in series are "off" and NAND output connect to Vdd because both parallel NMOS will on so n-out (AND output) connect to ground by which PMOS of right side will get "on" through the feedback path and connect the Vdd to out. The circuit shown below:

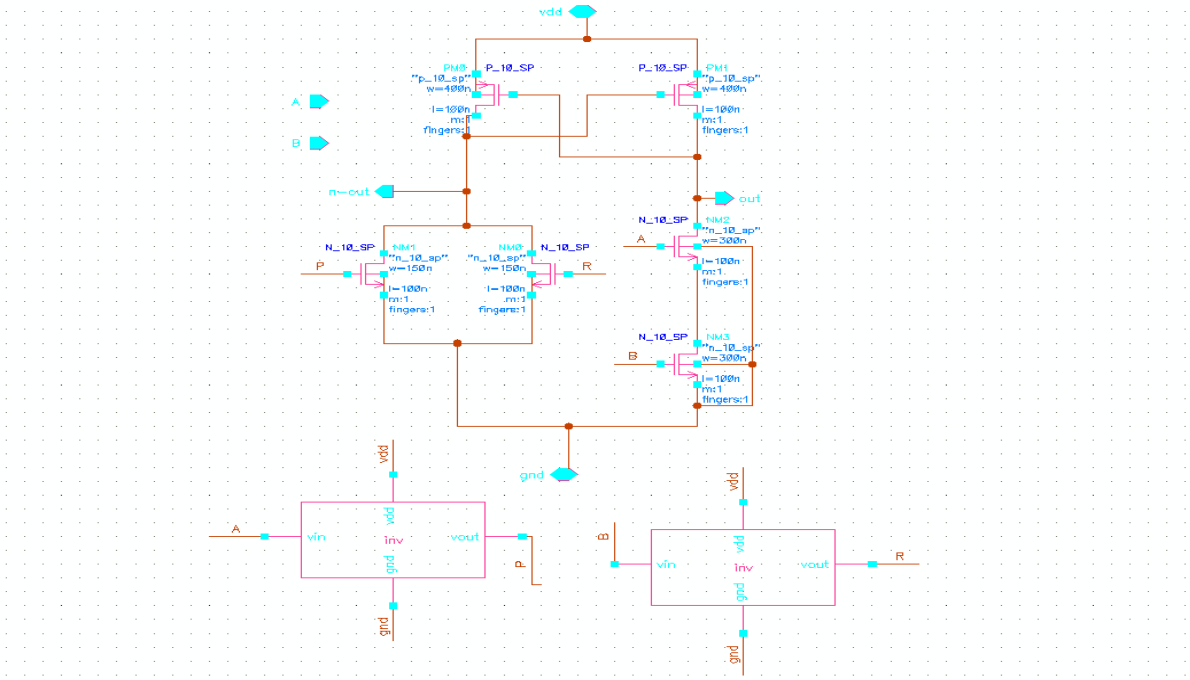



**Fig 6.1. Schematic AND gate using DCVSL [3]**

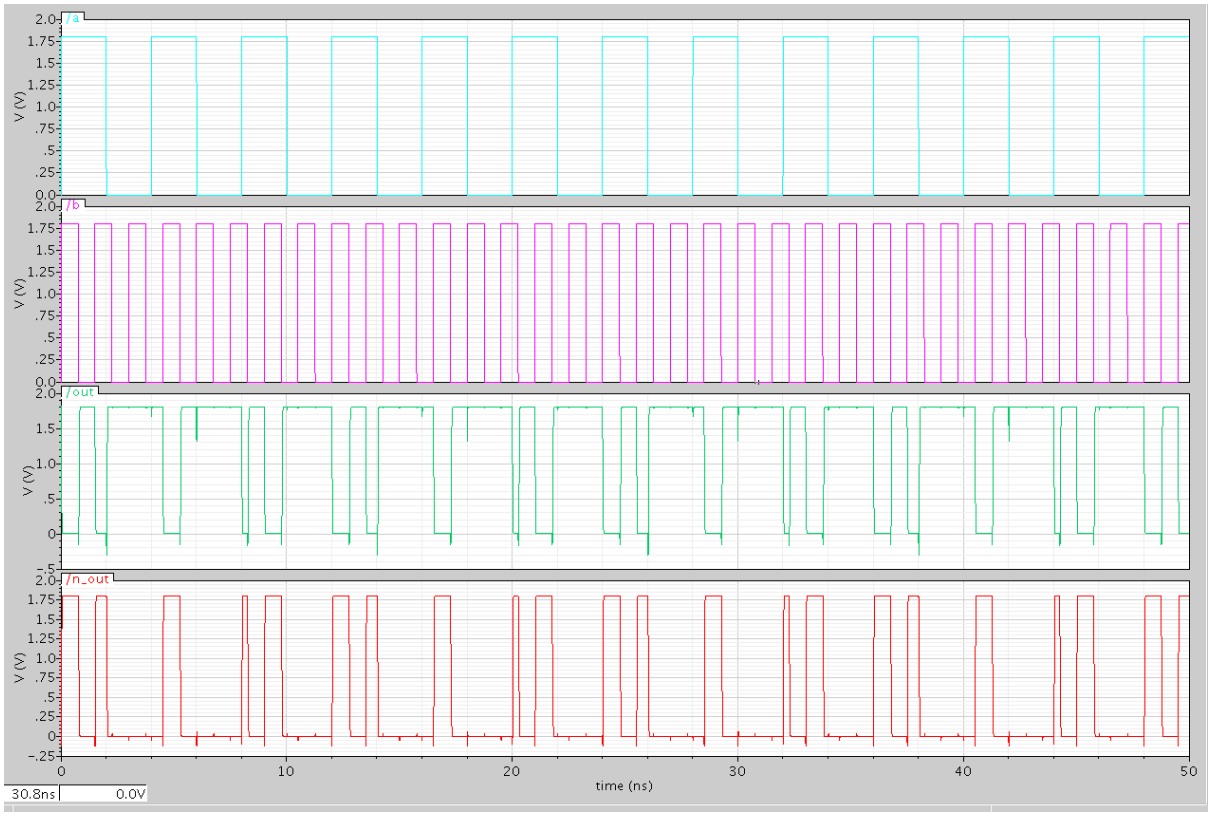



**Fig 6.2. Simulation of AND gate**

## 6.3. Design of D latch

We design the D latch using the “current mode logic” (CML). CML circuit having differential output so single stage will give two output which is inverse of each other. Because of the differential circuit this circuit very fast and it will improve the noise resistance.

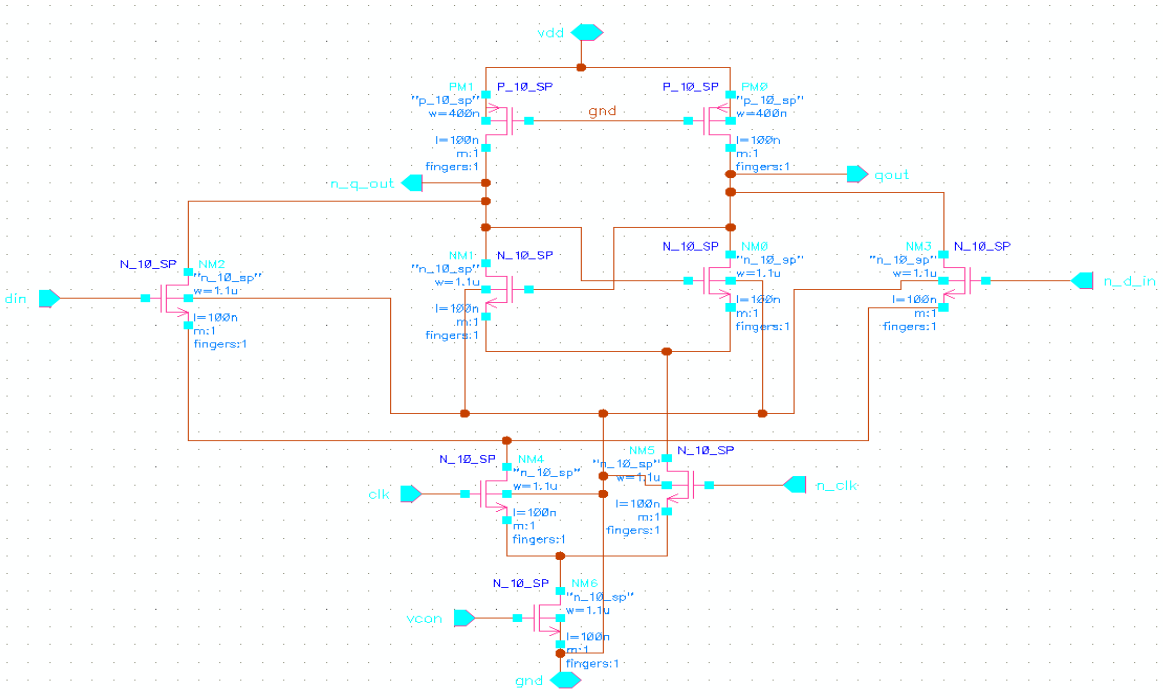



**Fig 6.3. Schematic of D latch using CML [3]**

When clk is high then output follow the input and when clk is low then latch hold the previous output, this is the definition of D latch. The circuit consist of an differential inputs (NM2 and NM3), a latch (NM1 and NM0) and clk pair (NM4 and NM5).

In sense mode, when clk is high then NM4 will get “on” and allowing NM2 and NM3 to sense the input and amplify the difference between the inputs. Which gives the output qout and

n_q_out. In latch mode, clk goes low then NM5 will get “on” and holding the last output by using the NM1 and NM0.

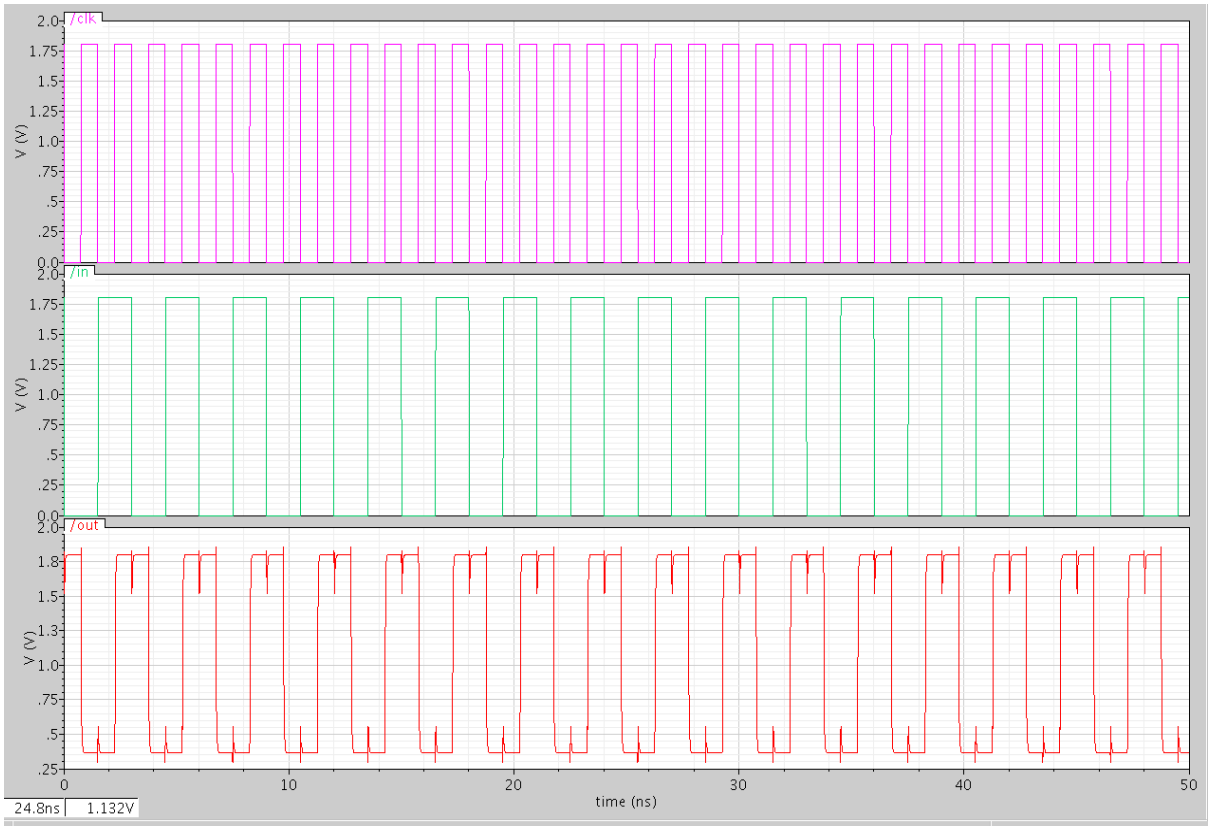



**Fig 6.4. Simulation of D latch using the CML**

## 6.4. Fractional divider

It is a circuit which divide the voltage controlled oscillator frequency by fractional number. The key word of this operation is “double edge triggered flip flop”. It having two D latch which is drive by clk and $\overline{clk}$ and a multiplexer.

### 6.4.1. Double edge triggered flip flop (DET)

DET flip flop having two latch driven by clk and $\overline{clk}$ and a multiplexer. As shown in fig.

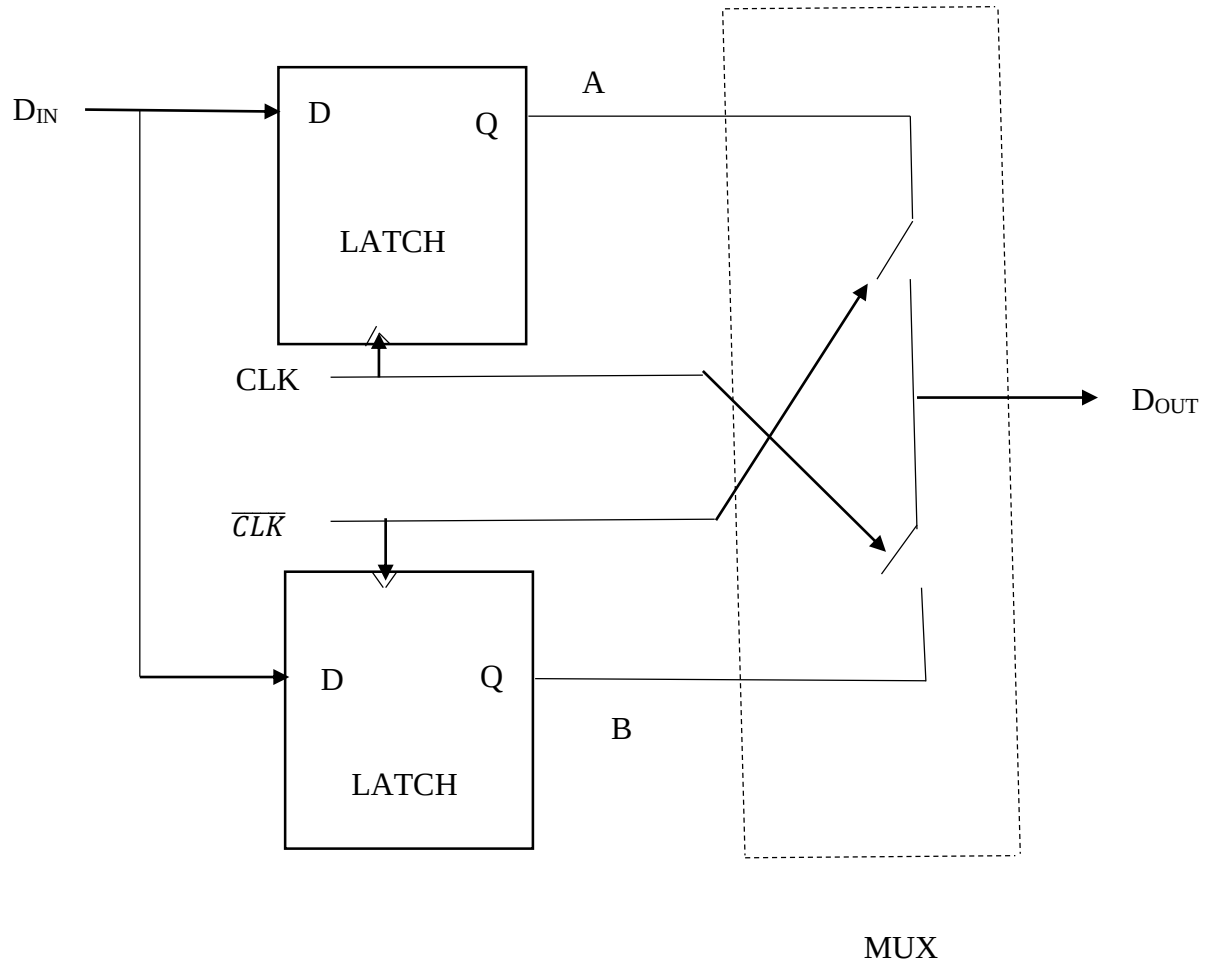



**Fig 6.5. Block Diagram of DET flip flop**

When clk is high, top latch is sense mode and bottom latch in the hold mode and vice versa. MUX select A when clk is low and select B when clk is high and give the output. we now drive the circuit with half rate clock, means now input having the period which is twice the original input bit period.

We can say that, for given clk rate, input data to DET flip flop can be twice as fast as that applied to a single D flip flop.

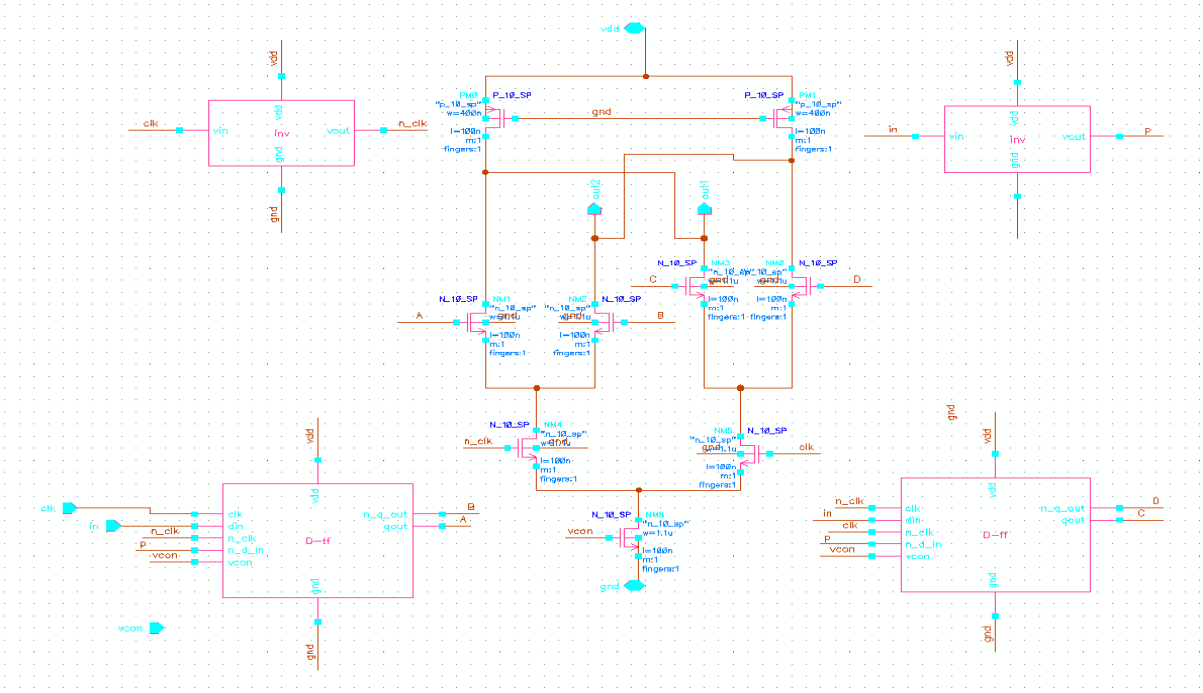


**Fig 6.6. Schematic of DET flip flop**

## 6.4.2. Divide – By – 1.5 circuit

In that circuit we are using the double edge triggered flip flop's and AND gate. This circuit read the input when clk is high and also when clk is low. It is circuit shown below

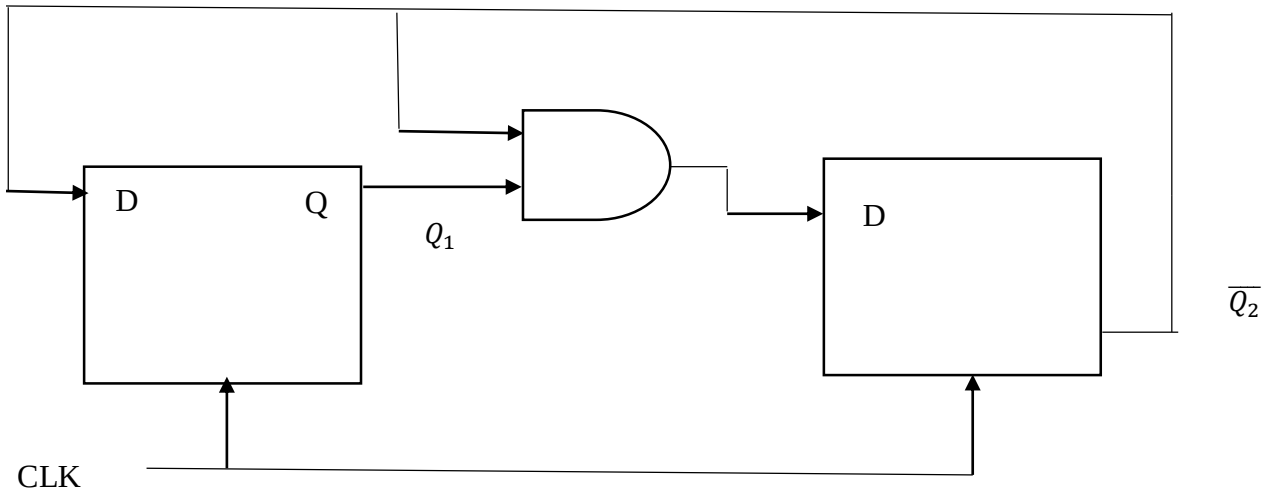



**Fig 6.7. Block diagram of 1.5 Divider**

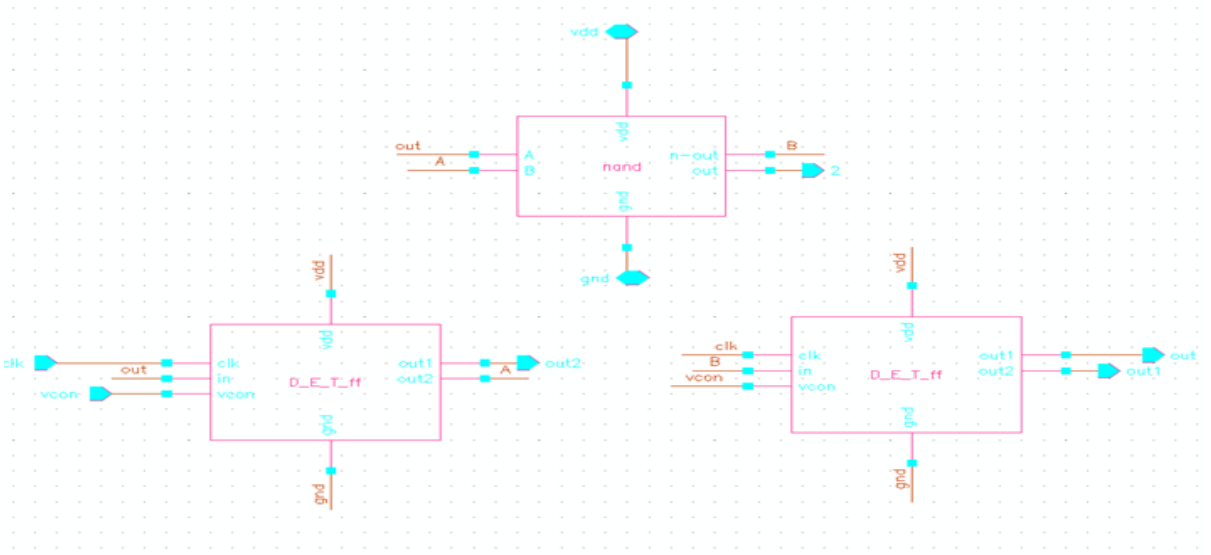



**Fig 6.8. Schematic of 1.5 Divider**

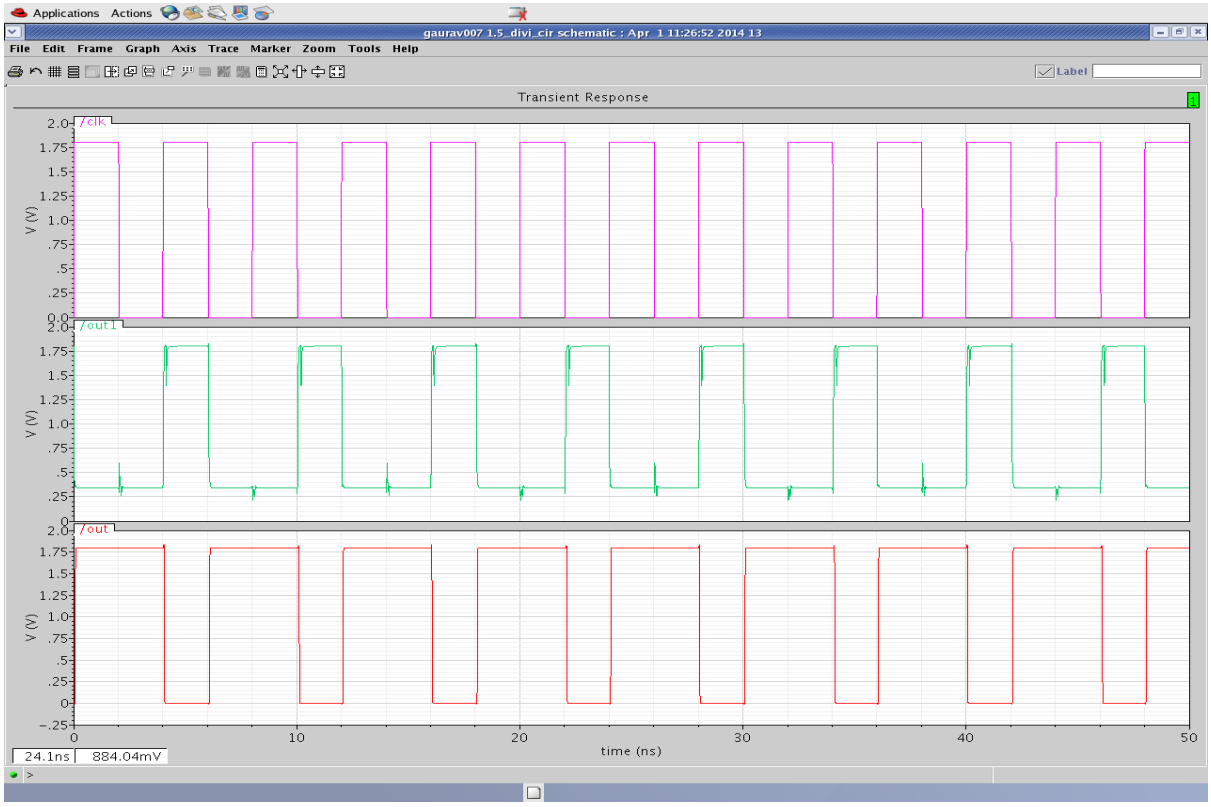



**Fig 6.9. Simulation of 1.5 Divider**

## 6.5. Phase locked Loop (PLL)

Phase frequency detector (PFD) compare frequency and phase of input signal with feedback signal. If there is a phase difference between the two signals then PFD generate the UP and DOWN signals. These signal increase/decrease the charge on filter. Then that charge speed up/slow down the frequency of VCO. There is loop filter which is low pass filter (LPF). LPF can pass only low frequency and stop the high frequency, so we can say that output signal from LPF is dc signals which drive VCO. When UP signal generated by PFD, then charge pump pumps the charge onto the LPF capacitor, which increase the $v_{control}$. By which the frequency of VCO will speed be up. When DOWN signal generated by PFD then charge pump remove the charge from the LPF capacitor, which decrease the $v_{control}$. By which the frequency of VCO will be slow down. The output signal with frequency $f_{VCO}$ is applied to divide by N.F circuit, which divide the $f_{VCO}$ By N.F and output signal of this circuit applied to PFD which compare these two signals, if phase error between these two signals is constant or zero then phase get locked. Then frequency of VCO ($f_{VCO}$) is N.F times the frequency of input signal.

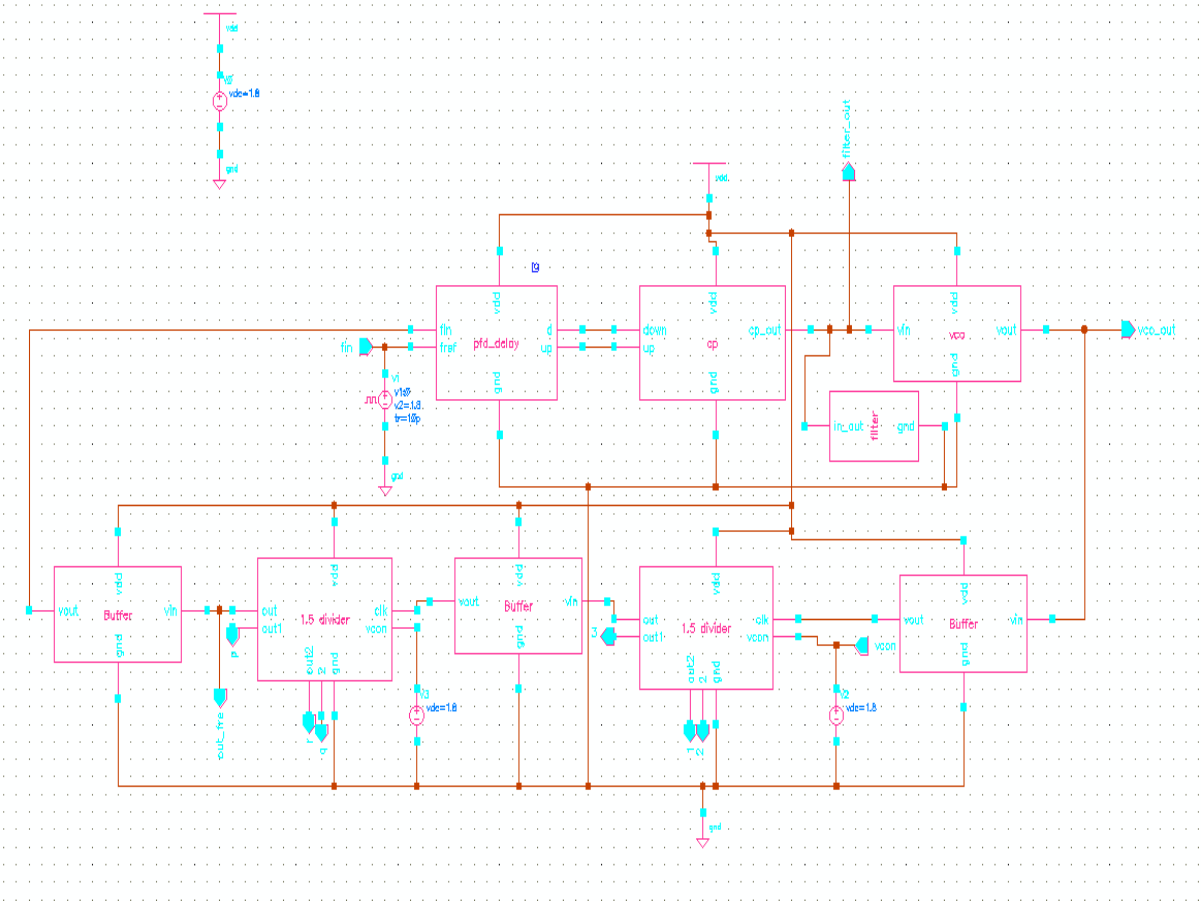



**Fig 6.10. Schematic of PLL as a Frequency Synthesizer**

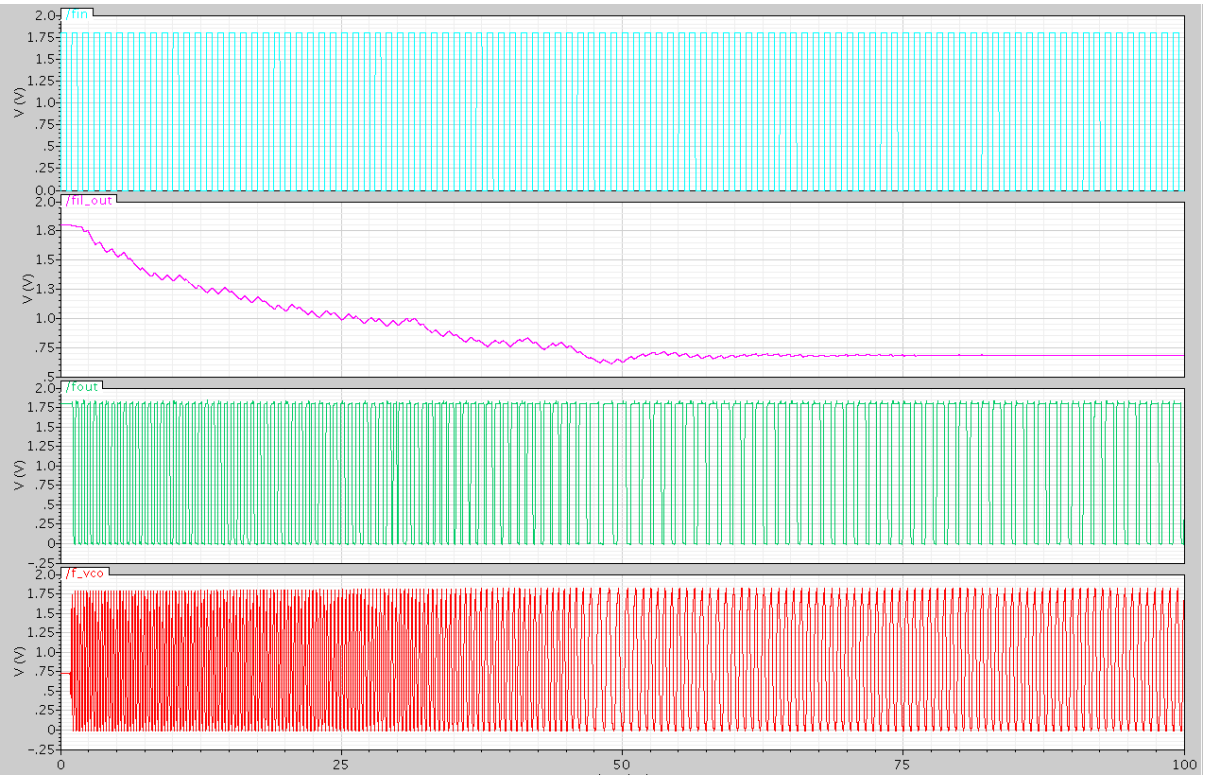



**Fig 6.11. Simulation of 1 GHz**

# CHAPTER 7

# CONCLUSION

## 7.1. Results

The lock time of Phase locked loop is 87.8ns and lock range is 1.175 GHz. The power dissipation of Phase locked loop is 5.3902mw at 1.5GHz and increase with the input frequency. The phase noise of phase locked loop is -99.9 dbc/Hz at 1.25GHz and increase with the frequency. The area of the layout of the PLL circuit is 0.00571 square micrometres. The centre frequency of voltage control oscillator is 2.5GHz.

## 7.2. Conclusions

The Phase locked loop is designed for a frequency multiplying factor of 2.25 and verified. The layouts of all the five blocks are draw and extracted each blocks. Then perform the post layout simulation. A new high speed PFD is proposed. In order to achieve the stability in loop filter we introduce a resister in series with capacitor. Current starved VCO is used as the voltage controlled oscillator in the design of Phase locked loop as a frequency synthesizer.

# REFERENCES


1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw-Hill Edition, 2002.

2. R.E.Best, "Phase-Locked Loops: Design, Simulation, and Applications”, 3rd edition, New York: McGraw-Hill, 1997.

3. Behzad Razavi, “RF Microelectronics”, Tata McGraw-Hill, 2nd edition, 1997.

4. Uma kanta nanda, “Design of a low noise PLL for GSM application”, IEEE International conference 2013.

5. Haripriya janardhan, MSEE Mahmud Fawzy Wagdy , “Design of a 1GHz Digital PLL Using 0.18µm CMOS Technology” , IEEE International conference 2006.

6. Adrang, "A Noval method for analysis and design of third-order charge pump PLL”, European Conference 2009.

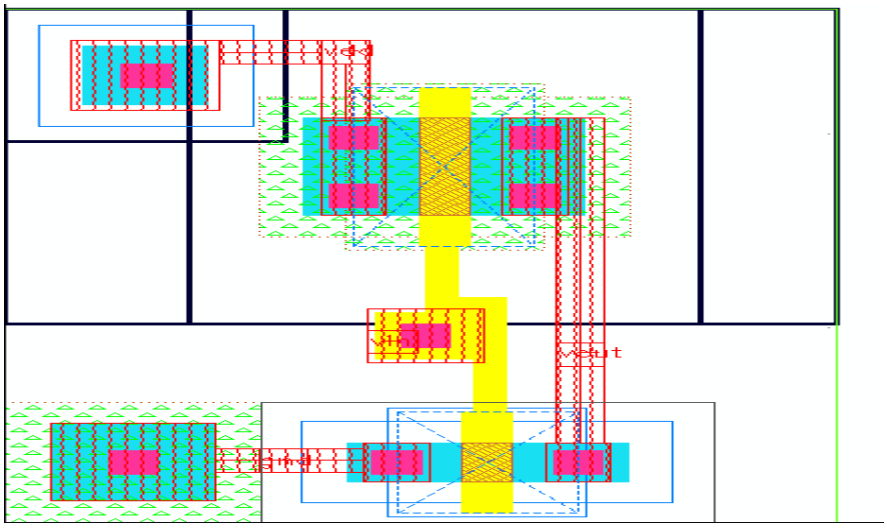
7. RJ.Baker, H.W.Li, and D.E.Boyce, "CMOS Circuit Design, Layout, and Simulation," IEEE Press Series on Microelectronic Systems, 2002.

8. G.B.Lee, P.K.Chan and L.Siek, “A CMOS Phase Frequency Detector for Charge Pump Phase Locked Loop”, 42nd Midwest Symposium on Circuits and Systems, Aug 8-11, 1999, volume 2, Page 601-604.

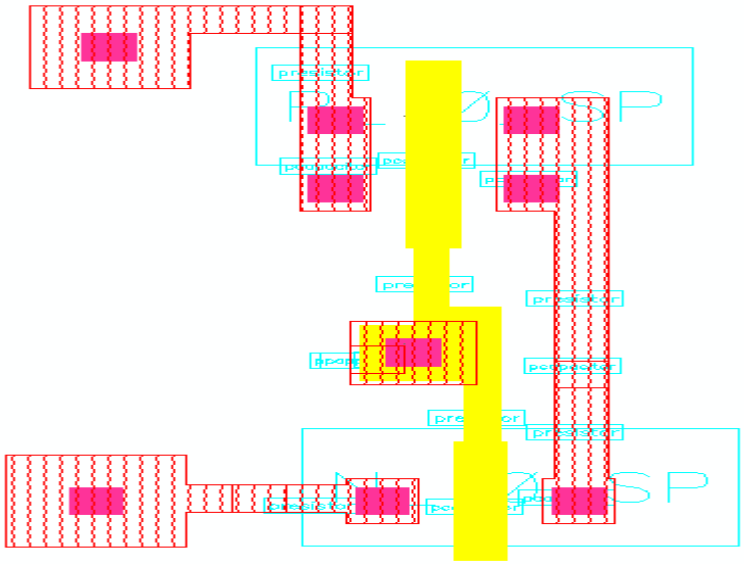
9. Yubtzuan Chen, Hong-Yu Huang, ―A Fast Acquisition CMOS Phase Frequency Detector‖, IEEE International Conference on Electro/Information Technology, May 7-10, 2006, Page 488-491.

10. P. Kinget, "A fully integrated 2.7V O.35um CMOS VCO for 5GHz wireless applications," IEEE International solid state circuit conference1998.

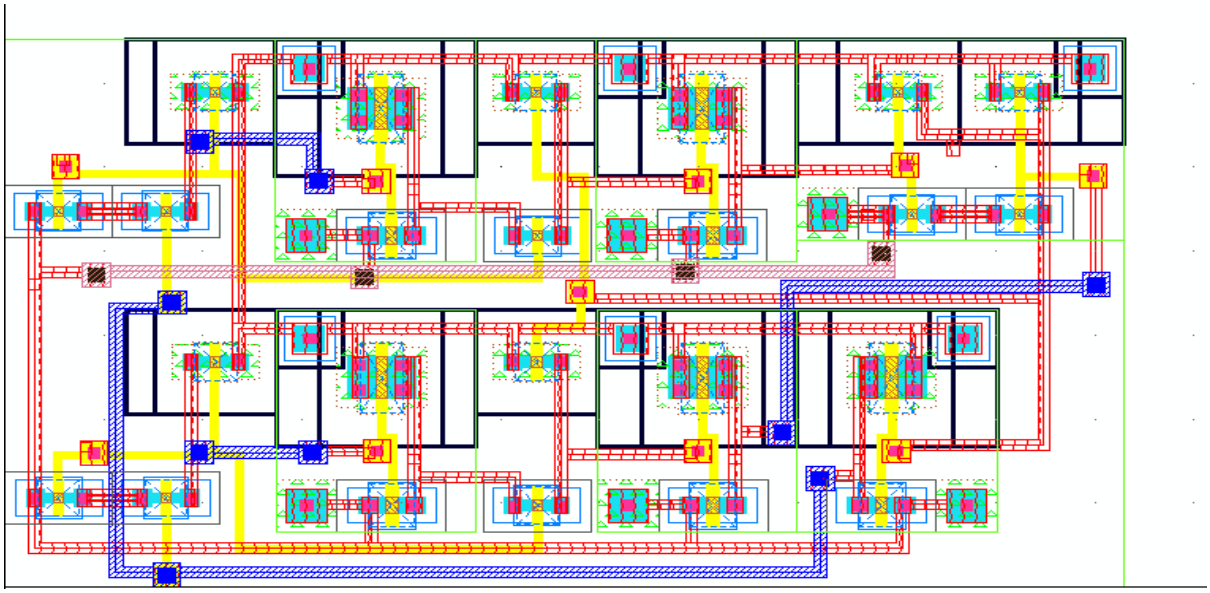
# Layouts



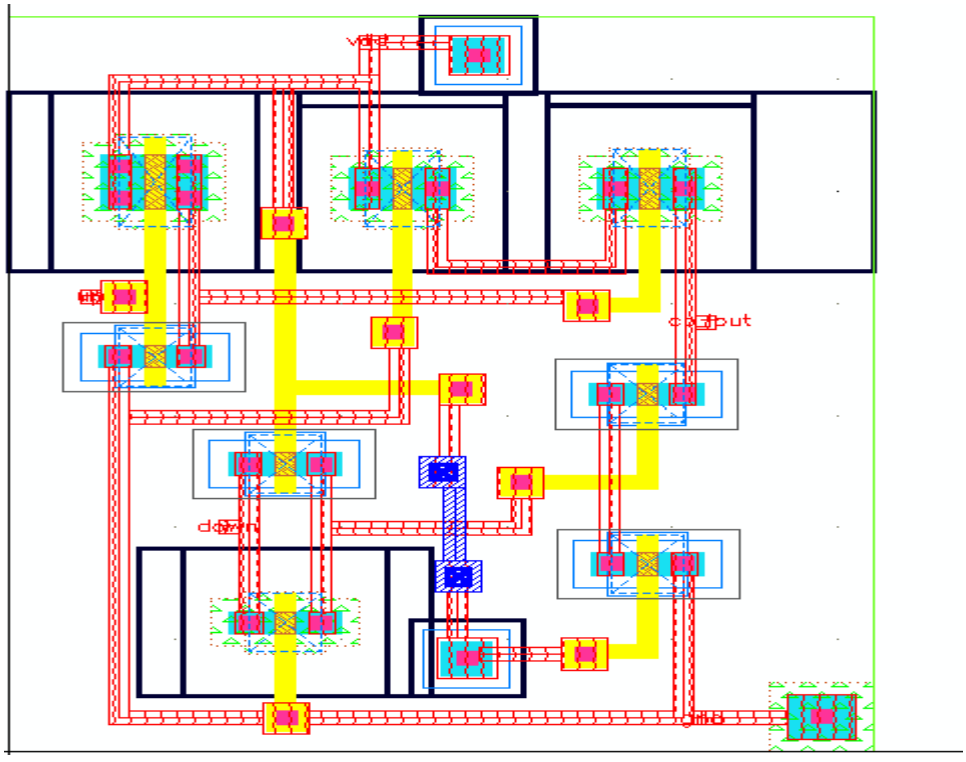
**Layout of inverter**



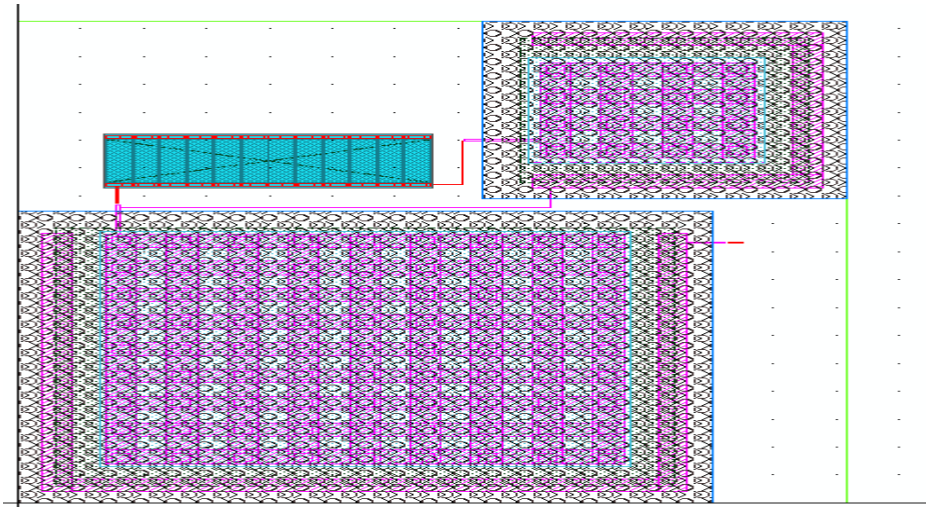
**Av_extracted of inverter**



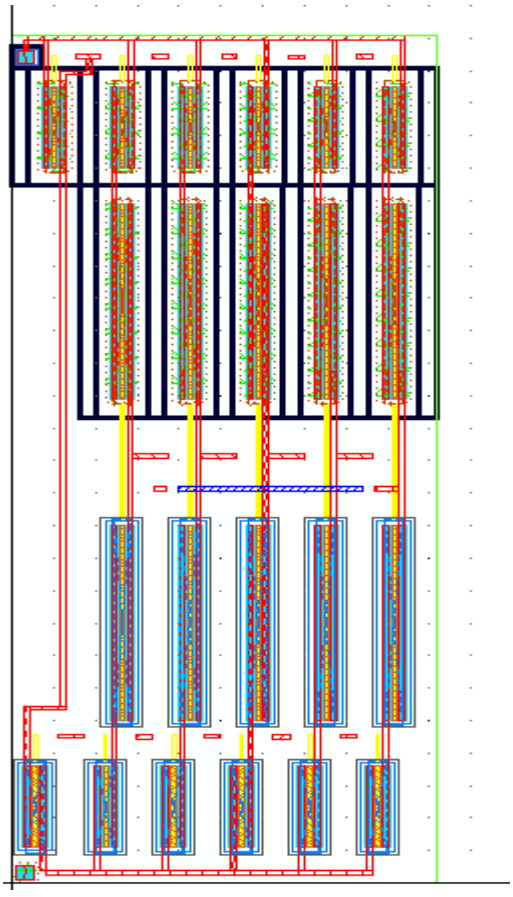
**Layout of PFD**



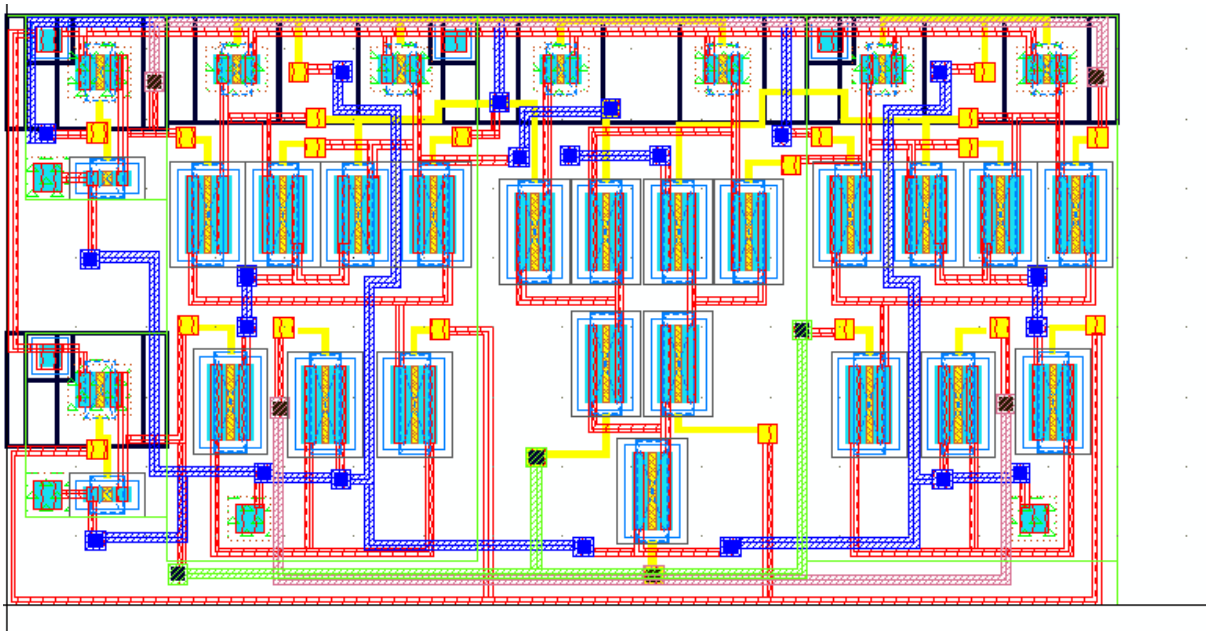
**Layout of CP**



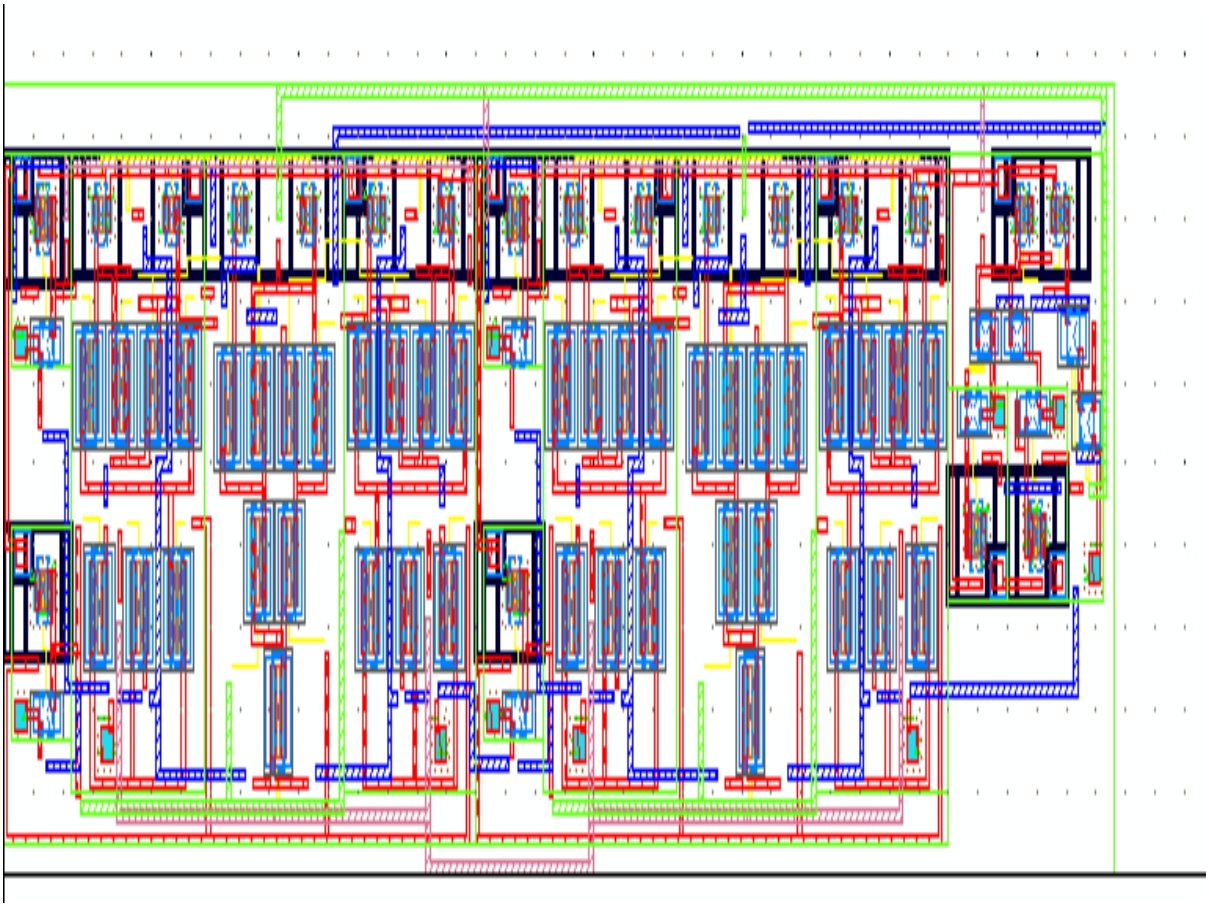
**Layout of loop filter**



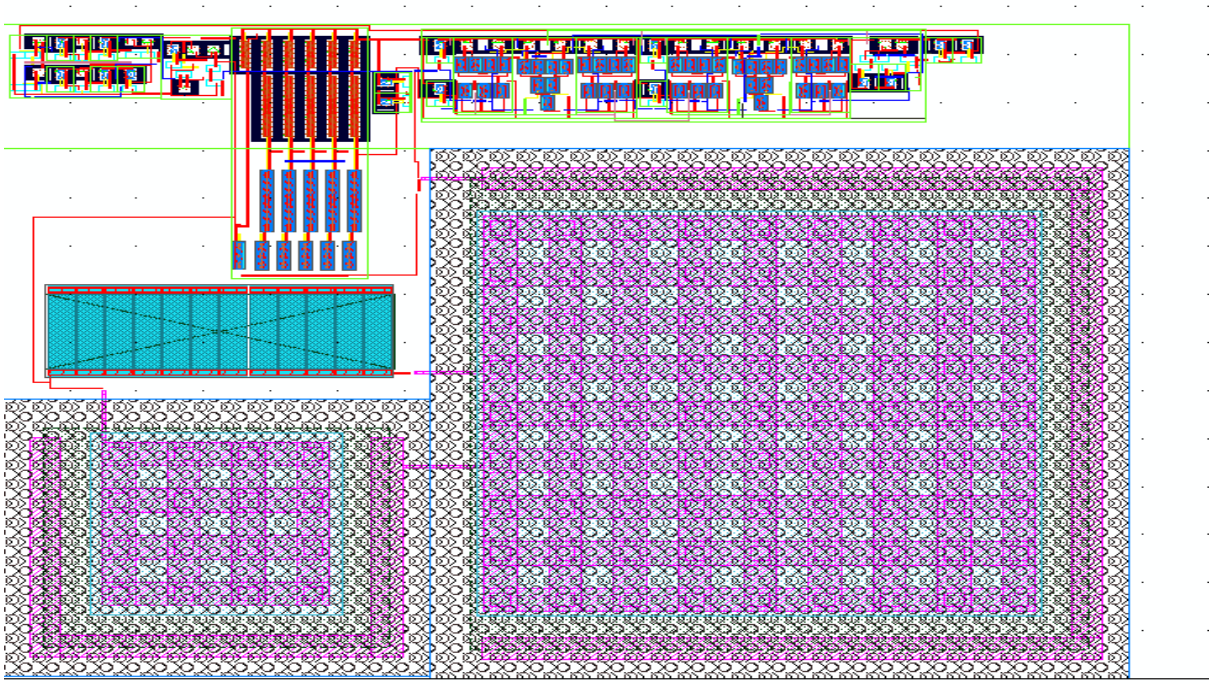
**Layout of VCO**



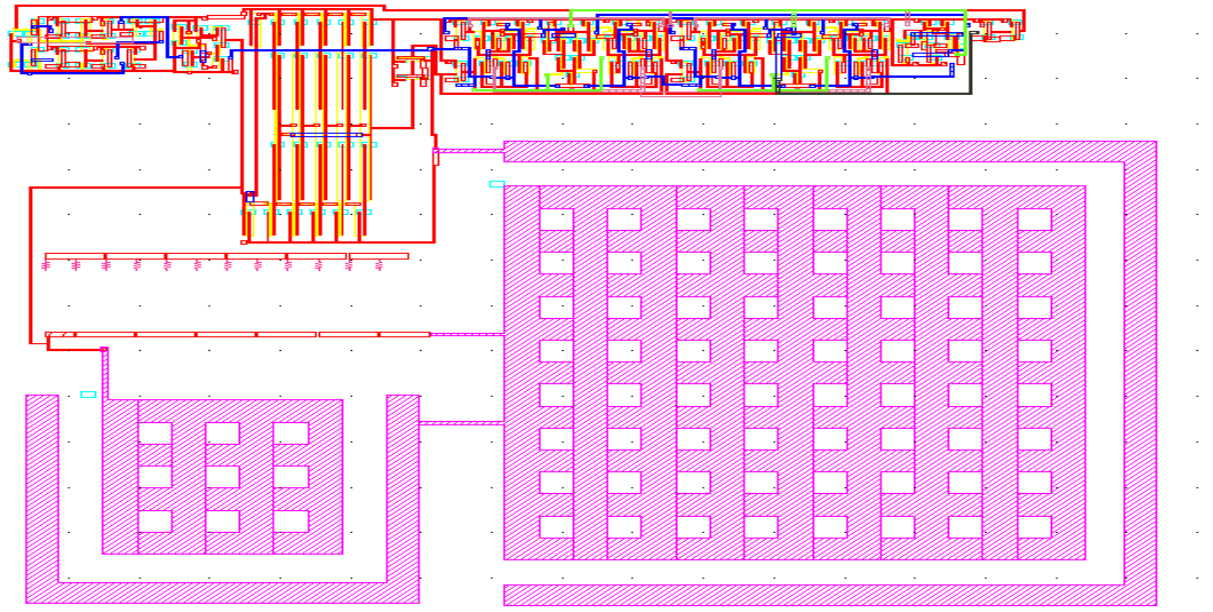
**Layout of D- E- T- FF**



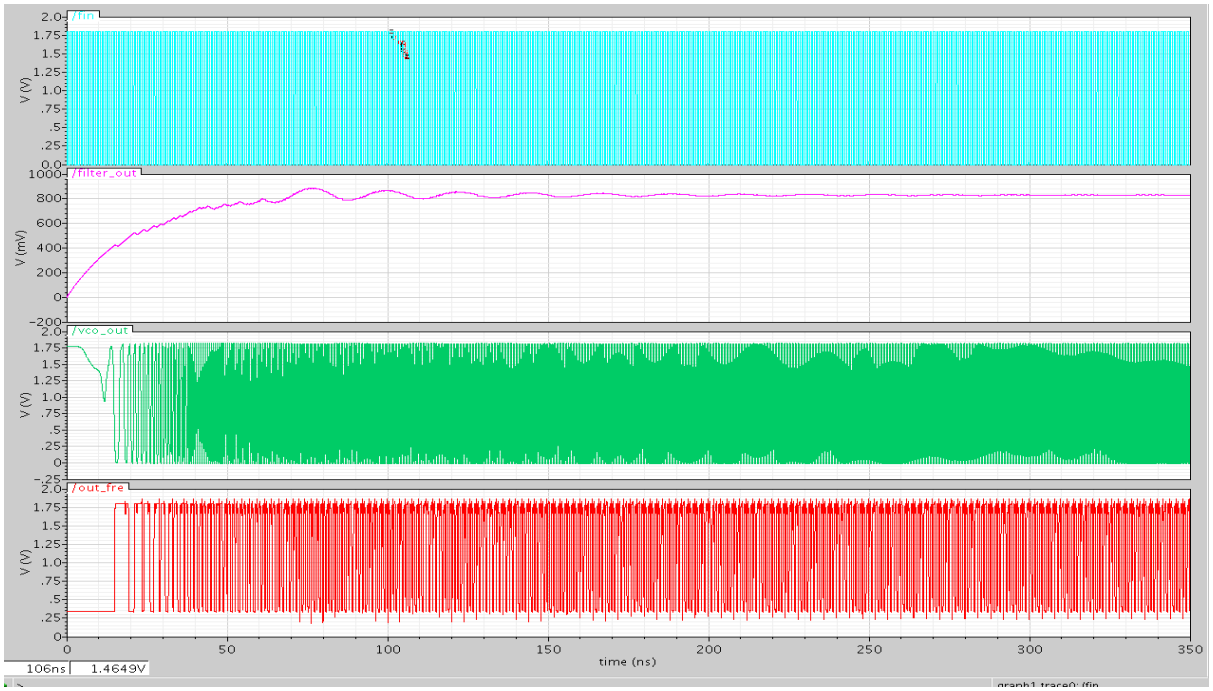
**Layout of 1.5 divider**



**Layout of PLL**



**Av_extracted of PLL**




**Post simulation of PLL**